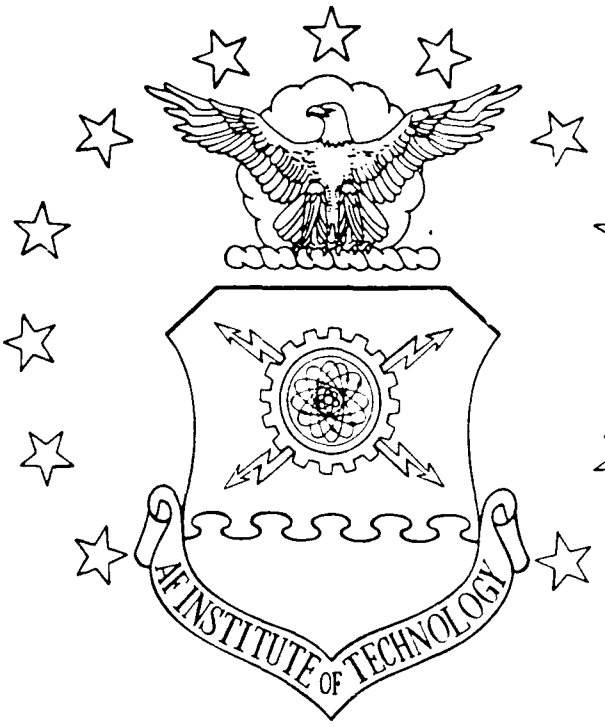

TESTING AND DATA PATH REDESIGN OF A HIGH SPEED, 16-POINT WINOGRAD FOURIER TRANSFORM PROCESSOR

THESIS

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Captain, USAF

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Approved for public release, distribution unlimited

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THESIS

Presented to the Faculty of tne Scool of Engineering

of the Air Force Institute of Technology

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In Partial Fulfillment of the

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Master of Science in Electrical Engineering

Steven W. Pavick, B.S.E.

Captain, USAF

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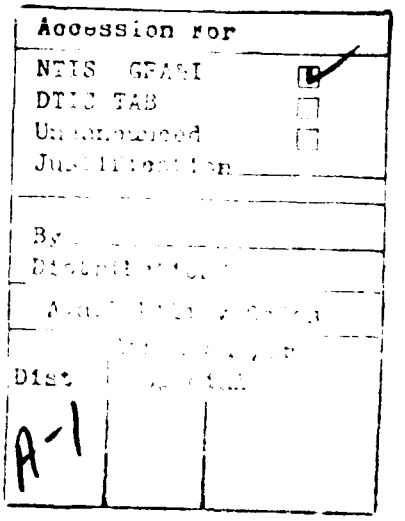
Most of all, I would like to thank my family for enduring my frequent and wide mood swings. Now my wife Sussan can have her husband back and the most special boys in the world, my sons Kristoffer and Oliver, have a daddy again.



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Abstract

A prototype 16-point, 70 MHz Fourier transform processor using 1.2 micron minimum feature sizes was tested using a Tektronix DAS 9200, digital analysis system. The results showed that it is possible to operate an Air Force Institute of Technology (AFIT) WFT16 chip at 70 MHz. The results also showed a great deal of variation among the individual packaged chips. Using the WFT16's built in testing circuitry, portions of the main data and control circuitry were tested. The AFIT XROM address generator and control circuitry proved to be the most reliable chip subsection, followed by the arithmetic and register control section. The parallel-in serial-out input data register was also tested and showed consistent results even though the results were not as expected. The variation among chips was shown when attempts at trivial transforms were done. The attempted transforms consisted of DC data values of zero and minus one. Two of 16 tested chips showed correct transform values, but for only a limited, nonrepeated sequence. In later testing, two chips were found that gave repeatable results which closely approximated the expected results for both trivial and nontrivial transform attempts. Test procedures and input to output relationships were determine to aid further testing of the AFIT WFT16 circuit.

1. Introduction

1.1 Background

Military synthetic aperature radars and other systems require discrete Fourier transforms of large amounts of data in near real time [Shepard, Rossbach]. These systems currently use multiple circuit cards inside expensive super computers in order to perform the required Fourier transforms. This existing technology is difficult to implement in airborne radar systems. In an effort to drastically scale down the existing methods of digitally performing Fourier transforms, research is being performed at the AFIT to use today's very large scale integration technology to implement a large scale digital Fourier transform (4030 data points) on a single computer card attached to a microprocessor. Although they currently furnish no funding, the Air Force Office of Scientific Research, the Wright Research and Development Center, and the Rome Air Development Center are interested in this project.

To fill the need for high speed Fourier transforms, AFIT instituted the WFTA project in 1984 which is aimed toward producing a working example of a high speed Fourier transform processing system using very large scale integration (VLSI) design techniques to implement the Winograd Fourier Transform Algorithm (WFTA) in either a single or a set of custom designed integrated circuits. The current goal is to produce

eight separate integrated circuits which work together to perform Fourier transforms using up to 4080 discrete points of data. The eight integrated circuits include three dynamic random access memories, one prime factor algorithm controller (the algorithm master controller), and three Fourier transform circuits [Lindermann].

Four AFIT thesis students, in 1985, selected the algorithms, hardware design, and integrated circuit technology to digitally compute a 4080-point discrete Fourier transform [Collins, Coutee, Rossbach, Taylor]. The selected algorithms are Winograd's Small Discrete Fourier Transform Algorithm, Winograd's Large Discrete Fourier Transform, and the Good-Thomas Prime Factor Algorithm [Taylor]. The integrated circuit technology selected was the standard 3-micron complementary metal-oxide-silicon (CMOS) technology using Manhatten (right angle only) geometries and MOSIS (an integrated circuit fabrication broker) design rules [Shepard].

In 1986, another AFIT thesis student followed on with the Wincgrad Fourier Transform Algorithm research by designing, simulating, and submitting to MOSIS for fabrication a 16-point Winograd Fourier Transform processor using 1.2-micron CMOS technology. This processor has been fabricated and returned to the Air Force Institute of Technology [Shepard].

As a class design project in 1988, two AFIT students designed and laid out the 17-point Winograd Fourier Transform

processor [Tillie].

1.2 Review of Current Liturature

This review was limited to the project work currently complete at AFIT. Even though other proposals for VLSI implementation of Fourier transform algorithms have been presented, they are not discussed in this thesis as they do not affect the direction or goal of this project.

1.2.1 Initial Design. In 1985, four AFIT Master's Degree Candidates undertook separate but related thesis projects. One student worked on establishing the overall basis for the 4080-point Fourier transform processor, while the other three limited the scope of their thesis projects to designing and verifying the hardware and architecture of the 16-point Winograd Fourier Transform Processor using the standard 3-micron integrated circuit design rules.

Captain Kent Taylor, USAF, examined different methods of doing discrete Fourier transforms before selecting Winograd's small and large discrete Fourier tranform algorithms. Taylor also developed the required implementation of the Good-Thomas Prime Factor Algorithm for the 4080-point prime factor algorithm processor and used C language computer simulations to verify the algorithms' accuracy [Taylor].

Working specifically with the 16-point Winograd Fourier Transform Processor were Captain Paul Rossbach, USA; Captain

Paul Coutee , UASF; and Captain Jim Collins, USAF. Rossbach designed the hardware used for the 16-point Winograd Fourier Transform Processor chip control and address generation [Rossbach]. Coutee designed the arithmetic architecture used to perform the 16-point Winograd Fourier Transform Processor transform [Coutee]. Collins developed a C language program that simulates the 16-point Winograd Fourier Transform Processor. Collins also wrote a VHDL simulation of some 16-point Winograd Fourier Transform Processor components [Collins].

1.2.2 Redesign. In 1986 three AFIT Master's Degree Candidates undertook thesis projects to refine the 16-point Winograd Fourier Transform Processor architecture and hardware, update the 16-point Winograd Fourier Transform Processor simulations, and design the prime factor algorithm controller, memory chips, and memory controllers required to integrate the entire 4080-point discrete Fourier tranform processor.

Captain Gary Hedrick, USAF, worked on the 4080-point discrete Fourier transform processor integration. He did the initial design of the prime factor algorithm controller as well as the memory chips and memory controllers required for the entire Winograd Fourier Tranform Algorithm processor to function properly [Hedrick].

Captain Carl Shephard, USAF, and Captain Chuck Cooper,

USAF, continued work on the 16-point Winograd Fourier Transform Processor. Shepard redesigned existing circuit macrocells, as well as doing original design on new macrocells, to update the 16-point Winograd Fourier Transform Processor circuit layout to conform with the new 1.2 micron process design rules. Cooper incorporated Shepard's new designs into the existing VHDL simulation [Cooper, Shephard].

In 1987, Lieutenant Robert Hauser, USAF, continued Hedrick's work of 1986. Hauser designed the memory chip and the Prime Factor Algorithm chip required to implement the 4080-point discrete Fourier transform [Hauser].

1.2.3 17-point Processor Design. In 1988, as a class project for an AFIT VLSI design course, Captain John Tillie, USAF, and Captain John Comtois, USAF, designed the 17-point Winograd Fourier Transform Processor chip. They modified existing macrocells used for the 16-point Winograd Fourier Transform Processor and designed new macrocells which were unique to the 17-point Winograd Fourier Transform Processor. They also worked on verifying their design [Tillie].

1.3 Current Problems Requiring Solutions

1.3.1 Testing. The 16-point Winograd Fourier Transform Processor has been fabricated and returned to the AFIT. This processor was tested using a computer event simulator prior to submission for fabrication. No testing had been done with any fabricated components of the processor, other than the XROM

and the associated address generation circuit, prior to fabrication.

1.3.2 Cell Library Organization. The WFTA cell library consists of approximatly 250 subcircuits. Each subcircuit is stored and manipulated using AFIT mainframe computers. Each subcircuit occured at least three times within the directory structure of AFIT's Galaxy computer, twice within the BSD computer and once within the Ares system of Sun4 computers.

1.3.3 Cell Design Rule Errors. After the WFTA16 was submitted for fabrication, MOSIS issued a change to the fabrication design rules for the 1.2-micron, scalable CMOS process used. These changes resulted in the appearance of numerous fabrication design rule errors where transistor gate and drain diffusions did not meet the mimimum requirements for froming those areas on either side of the polysilicon base. Table 1-1 shows the results of the rule change.

1.3.4 Documentation. The documentation of the WFTA research effort is contained in seven related theses. These theses have emphasized what was done and what was the resulting end product. The specifics, on why and how decisions were made are not included in the final reports. In addition, microcell design documentation consists of simple abstract block diagrams.

Table 1-1: Design Rule Error Count for WFTA Subcells.

Cell Name	Total Cell Occurances	Dimensions (lambda)	Errors per Cell	Error Density ($1000\ err/cm^2$)
piso_cell_L	32	77 x 120	1	30.1
addmsff	48	39 x 133	2	107.1
addsubmod	80	132 x 222	11	104.3
addcon	12	83 x 222	3	45.2
Rmult0a	14	87 x 429	3	22.3
Rmult0	2	87 x 429	5	37.2
Rmultp1a	8	87 x 429	9	67.0
Rmultn1a	12	87 x 429	18	134.0
Lmult0a	16	87 x 402	3	23.8
Lmult0	4	87 x 402	2	15.9
Lmultp1a	8	87 x 402	9	71.5
Lmultn1a	8	87 x 402	6	47.7
mult0a	196	87 x 297	7	75.3
mult0	52	87 x 297	8	86.0
multp1a	66	87 x 297	13	139.8
multn1a	68	87 x 297	15	161.3
multp2a	18	87 x 297	17	182.8
mult2n	16	87 x 297	11	118.3
multcon	24	80 x 297	2	23.4
rmultcon	2	80 x 297	2	23.4
mult_inv	26	104 x 297	1	11.7
parrnd_cell	32	81 x 367	1	9.3
sipo_cell	690	81 x 125	1	27.4
sipo_cell_D	46	81 x 125	4	109.7
sipo_cell_DMSB	2	83 x 135	3	74.4

Note: 1 lambda = 0.6 micron

1.4 Proposed Solutions to Problems

1.4.1 Testing. Testing of the fabricated 16-point processor will be done with the Tektronix DAS 9200, Digital Analysis System, and its associated equipment. The test plans

found in the Shephard thesis will be followed as much as possible.

This promises to be the most challenging aspect of this thesis effort as the required equipment is still relatively new to the AFIT and the manufacturer's documentation on system operation consists of disjointed facts tied together without examples of or insight into actual operations.

1.4.2 Cell Library Improvements. The existing file structure will be checked for all correct files required to make up the basic WFTA and extended WFTA16 cell libraries. All basic cells required for WFTA arithmetic operations will be simulated, analyzed, and redesigned. The data gathered from this will be combined with all pertinent cell data, such as control and data signals, in such a way that another engineer can quickly determine the operations and purpose of each subcircuit. A new computer file structure will be set up in which subcircuits will be logically grouped together. Only subcircuits with the correct logic implemetaion will be kept and the other occurrences will be deleted.

Once the new organization has been completed, it will be backed up on tape and be kept on AFIT's Ares Sun4 system.

1.4.3 Cell Library Verification. All existing arithmetic subcells will be checked for design rule errors and those errors will be eliminated. During the redesign process,

cell size minimization will also take place. Also test chips will be designed for fabrication in order to physically charactorize the new subcells.

2. WFTA16 Chip Testing

2.1 Introduction

Forty-eight packaged WFTA16 integrated circuit chips were fabricated through MOSIS. Of these, four were rendered useless prior to this testing effort when power and ground signals were accidently applied to the wrong circuit pins, leading to a short between a power pad and a clock pad, causing a bonding wire to break. Of the remaining chips, 12 were not used in any way for testing and were set aside for possible future work.

Two basic kinds of testing were performed. First a DC check was performed to check for power shorted to ground, then functional tests were run to determine whether the WFTA16, as fabricated, functioned correctly.

The Tektronix DAS 9200, Digital Analysis System, and associated equipment were used to perform all functional tests. This equipment was initially designed as a logic analyzer then adapted to a device verification function. The features and shortcomings of this equipment are discussed later.

2.2 DC Tests

All of the remaining 32 WFTA16 chips were tested for shorts between power and ground. Each of the tested WFTA16 packages were uniquely identified by either a letter or combination of letters and a number. Those chips with "GND"

in their name had a extra bonding wire added after AFIT received the chips to apply chip ground directly to the chip's substrate. This wire was added as the only substrate to ground connections were well contacts within subcells. During testing, these chips showed no differences from the other chips. The chips marked "OXIDE" were used for simple probe tests of the input/output pads to determine that the pins were electrically connected to the pads and that the top oxide layer over the pads was etched off correctly during fabrication.

This test checked for short circuits between the power and ground inputs. A nine volt digital ohmmeter was used to determine the resistance between the power and ground pins. The results of this test are summarized in table 2-1.

Table 2.1: Resistance measurements between power and ground pins of WFTA16 integrated circuit chips.

Chip Label	Measured Resistance	Chip Label	Measured Resistance	Chip Label	Measured Resistance
A	156.9 ohm	L	10.6 Mohm	W	17.3 ohm
B	554.0 ohm	M	64.8 ohm	X	14.1 chm
C	8.8 Mohm	N	188.4 ohm	Y	9.5 Mohm
D	10.3 Mohm	O	8.7 Mohm	#1 OXIDE	9.0 Mohm
E	10.3 Mohm	P	28.7 ohm	#2 OXIDE	10.2 Mohm
F	95.6 ohm	Q	8.8 Mohm	#3 OXIDE	10.6 Mohm
G	9.4 Mohm	R	10.2 Mohm	GND-1	3.1 Mohm
H	10.7 Mohm	S	10.5 Mohm	GND-2	8.7 Mohm
I	9.3 Mohm	T	7.6 Mohm	GND-3	25.1 ohm
J	8.8 Mohm	U	9.0 Mohm	GND-4	10.4 Mohm
K	8.7 Mohm	V	64.2 ohm		

The 10 chips found to have resistances below the kohm level were removed from further testing. These failures represent a 31% failure rate. Six of the remaining chips (J, K, L, O, Q, and R) were then set aside for any future testing beyond that accomplished in this thesis. The 16 remaining chips were then tested using the Tektronix DAS 9200, Digital Analysis System.

2.3 Functional Testing

2.3.1 WFTA16 Test Structure. The WFTA16 was designed to incorporate a high degree of testability. The structures and logic used to facilitate testing are included in the Shephard thesis, chapter 3 and appendix.

The basic test structures are an 18-bit input bus, 18-bit output bus, and a PLA. The input bus is used to deliver data from the RPISO07 through RPISO24 pins to the preadder, multiplier, postadder, or SIPO register functional areas depending on the test mode selected. The output bus takes the results from the PISO register, preadder, multiplier, or postadder functional areas to the RSIPO07 through RSIPO24 or ISIPO07 through ISIPO24 output pads depending on whether the data was generated within the real or imaginary arithmetic sections and on the test mode selected. The PLA is used to select the chip's functional areas for testing.

2.3.2 Equipment. The primary piece of equipment to test the WFTA16 was the Tektronix DAS 9200 and associated

equipment. The DAS 9200 system consists of a computer keyboard and color monitor workstation attached to a CPU. The CPU controls upto 8 TTL acquisition probe pods and 8 TTL stimulus probe pods. Each of the acquisition probe pods have 8 probe tips for sensing the output pin voltage levels of the device under test. The stimulus probe pods have 8 probe tips to supply data to the device under test as well as a stobe line to provide the required chip clocks. All probe pods and probes are attached to the under side of a TF 100 unit and make connection with the device under test (DUT) through a device socket card on which the DUT is mounted.

The DAS 9200 uses a menu driven software approach to select operating parameters such as operating frequency and chip clock pulse width. When being used in its device verification functions, the DAS 9200 will operate only at preprogrammed frequencies from 1 kHz to 50 MHz. The chip clock parameters are also limited to a preprogrammed selection.

Test vectors are stored in a pattern file that contains the values assigned to the chip data and clock input pins, as well as, the data expected to be output from the chip. Again, the test pattern is set up using a menu driven software approach. The test vectors are the results of circuit simulations done prior to testing using the DAS 9200.

Once the test pattern is set up and the operating

parameters are selected, a test can be run. This test takes the operating parameters to set up both the system and chip clocks, then steps through the test pattern while acquiring the chip output data. After the pattern is finished, the acquired data is compared to the expected data and error messages are displayed. The errors are displayed within the pattern file where a red expected data value signifies an unexpected result was obtained.

2.3.2.1 Equipment Setup. All probe pods and tips were mounted to the underside of the TF 100. This took advantage of the automatic routing of stimulus and acquisition lines to the probe collar around the center of the TF 100. In order to get the probes connected to the chip, a device socket card was required. This required wiring from points near the edge of the card, where it made contact with the TF 100 probe collar, to the center of the card where the DUT is placed. Instead of wiring directly to a WFTA16 package, a zero insertion force (ZIF) socket was placed in the middle of the device socket card and the wires were soldered to it. During testing, each DUT would then be placed within the ZIF socket

After testing began, a series of plastic cams broke within the ZIF socket. This resulted in the inability of one half of the socket to open in order to accept a device for testing. This problem was overcome through the use of a prototype 144 pin grid array (PGA) using low insertion force

pin acceptors. The 144 PGA was forced into the ZIF socket. Test chips were then placed in the PGA for testing.

With the 144 pins of the WFTA16 chip, it was necessary to assign each pin a name. Most pins were assigned unique names based on pin purpose. The following explains the assigned pin names:

Power

Vdd - Common chip voltage supply input. Occurs four times.
GND - Common chip ground. Occurs four times.

Clocks

PQ1_C - First phase of the duel phased non-overlapping clock. This clock is independent from all other clocks and affects the control section only.
PQ1_DR and PQ1_DI - First phase of the duel phased non-overlapping clock. This clock is independent from all other clocks and affects the arithmetic and register sections only. These two pins are hard wired together on chip.
PQ2_C - Second phase of the duel phased non-overlapping clock. This clock is independent from all other clocks and affects the control section only.
PQ2_DR and PQ2_DI - Second phase of the duel phased non-overlapping clock. This clock is independent from all other clocks and affects the arithmetic and register sections only. These two pins are hard wired together on chip.

Control Data

OPR - Chip operate. This pin must be high inorder to place the chip in an operational mode.
LD - Load scaling factor and test modes. This signal must be high to load the scaling factor data from the scaling and state data pins on to the chip so the correct number of sign extensions ans zerofills can be added to each data word. It also loads the test state from the RSIP001 to RSIP004 pins when high. When low, along with OPR being low, the DFT size and watchdog controls are loaded from the scaling and state data pins.
TEST - Enter test mode. When high, this signal

activates the test bus structure to perform the test associated with the data loaded while LD was last high.

Scaling and State Data

SF2 - Scale MSB/Watchdog. This signal represents the MSB of the three bit scale factor and the watchdog state bit. When LD and OPR are low and this bit high, the chip is placed in watchdog mode.

SF1 - Scale middle bit/DFT size MSB. This signal represents the middle bit of the three bit scale factor and the MSB of the two bit DFT sizing word.

SF0 - Scale LSB/DFT size LSB. This signal represents the LSB of the three bit scale factor and the LSB of the two bit DFT sizing word.

Input Data

RPISO01 to RPISO24 - Real data input word. This word represents the 24-bit data word input to the real side of the WFTA16 processor. The data input through RPISO24 is the data parity bit used to ensure odd parity.

IPISO01 to IPISO24 - Imaginary data input word. This word represents the 24-bit data word input to the imaginary side of the WFTA16 processor. The data input through IPISO24 is the data parity bit used to ensure odd parity.

Output Data

RSIPO01 to RSIPO24 - Real data output word. This word represents the 24-bit data word output from the real side of the WFTA16 processor. The data output through RSIPO24 is the data parity bit used to ensure odd parity.

ISIPO01 to ISIPO24 - Imaginary data output word. This word represents the 24-bit data word output to the imaginary side of the WFTA16 processor. The data output through ISIPO24 is the data parity bit used to ensure odd parity.

Data Addressing

IA1 to IA12 - Input data memory address. This chip generated word specifies the memory data location from which input data words are to be read.

OA1 to OA12 - Output data memory address. This chip generated word specifies the memory data location to which output data words are to be written.

Chip Status

DONE - Processing complete. This chip generated signal raises when the last data words are written.
PE - Input parity error. This signal goes high if the on chip parity detection circuit senses an input data word with an even parity.
WDE - Watchdog mode error. When the chip is in watchdog mode, the chip's outputs are disabled but compared with the outputs of an active chip. If a difference is detected during processing this signal will raise.
WE - Write enable. Controls memory access.

With 54 input, 75 output, 6 clock, 4 ground, and 4 power signals associated with each WFTA16 chip, the wiring of the device socket card was quite complicated. The chip power and ground pins were wired to predesignated positions on the device socket card, while the probes could be wired to any available probe position on the TF 100. The 54 input pins and four clock pins used were assigned stimulus probes as shown in table 2.2. Since the maximum number of probes available to sense data from the chip was 64, not all outputs could be sensed. Table 2.3 shows the output wiring assignments.

2.3.2.2 DC Probe Voltage Biasing. The stimulus probes used with the DAS 9200 use TTL voltage levels. As such, the low voltage, or logical zero, is 0.7V higher than the low voltage used to power the probe and the high voltage, or logical one, is 0.7V lower than the high voltage used to power the probe. The probes have another draw back in that they are fused such that if a voltage differential greater that 5.2V is input, then the fast acting fuses blow.

Table 2.2: WFTA16 input pin to DAS 9200 stimulus and clock probe position assignment and reference clock wiring.

Signal Name	Pin #	Probe Point	Signal Name	Pin #	Probe Point	Signal Name	Pin #	Probe Point
Real Data			Imaginary Data			Control Data		
RPISO01	39	3-2	IPISO01	142	11-7	OPR	28	5-0
RPISO02	40	3-4	IPISO02	141	11-6	LD	32	3-0
RPISO03	41	3-5	IPISO03	140	11-2	TEST	33	3-1
RPISO04	42	3-3	IPISO04	139	11-3			
RPISO05	43	3-7	IPISO05	138	11-4			
RPISO06	44	3-6	IPISO06	137	11-1	Scaling and State Data		
RPISO07	45	1-1	IPISO07	136	11-0			
RPISO08	46	1-2	IPISO08	135	13-5			
RPISO09	47	1-0	IPISO09	134	13-6	SF0	29	5-3
RPISO10	48	1-5	IPISO10	133	13-2	SF1	30	5-1
						SF2	31	5-2
RPISO11	49	1-4	IPISO11	132	13-7			
RPISO12	50	1-3	IPISO12	131	13-3			
RPISO13	51	1-6	IPISO13	130	13-1			
RPISO14	52	31-1	IPISO14	129	13-0			
RPISO15	53	31-0	IPISO15	128	15-7	Clocks		
RPISO16	54	1-7	IPISO16	127	13-5	PQ1_C	35	3 8
RPISO17	55	31-2	IPISO17	126	15-6	PQ1_DR	73	31-8
RPISO18	56	31-3	IPISO18	125	15-4	PQ2_C	36	5-8
RPISO19	57	31-7	IPISO19	124	15-5	PQ2_DR	70	29-8
RPISO20	58	31-4	IPISO20	123	15-1			
RPISO21	59	31-6	IPISO21	122	15-0			
RPISO22	60	31-5	IPISO22	121	15-3			
RPISO23	61	29-0	IPISO23	120	15-2			
RPISO24	62	29-1	IPISO24	119	11-5			

Reference Clock Wiring Connections

Reference Stimulus Clock:	13-8
50% Duty Cycle Acquisition Clock:	21-CLK
Return to Zero Acquisition Clock:	7-8

Table 2.3: WFTA16 output pin to DAS 9200 stimulus probe position assignment.

Signal Name	Pin #	Probe Point	Signal Name	Pin #	Probe Point	Signal Name	Pin #	Probe Point
Real Data			Imaginary Data			Input Data Memory Address		
RSIPO01	63	17-3	ISIPO01	118	17-6	IA1	2	9-2
RSIPO02	64	27-0	ISIPO02	117	17-7	IA2	3	9-0
RSIPO03	65	27-1	ISIPO03	116	17-2	IA3	4	9-4
RSIPO04	66	27-3	ISIPO04	115	17-4	IA4	5	9-7
RSIPO05	67	27-4	ISIPO05	114	17-0	IA5	6	9-1
RSIPO06	68	27-2	ISIPO06	113	17-5	IA6	7	9-6
RSIPO07	69	27-5	ISIPO07	112	19-2	IA7	8	9-3
RSIPO08	74	27-6	ISIPO08	107	19-5	IA8	9	7-2
RSIPO09	75	27-7	ISIPO09	106	17-1	IA9	10	7-1
RSIPO10	76	25-2	ISIPO10	105	19-7	IA10	11	9-5
RSIPO11	77	25-5	ISIPO11	104	19-1	IA11	12	7-3
RSIPO12	78	25-0	ISIPO12	103	19-4	IA12	13	7-4
RSIPO13	79	25-4	ISIPO13	102	19-6			
RSIPO14	80	25-1	ISIPO14	101	19-3			
RSIPO15	81	23-1	ISIPO15	100	19-0			
						Status Bits		
RSIPO16	82	25-7	ISIPO16	99	21-5			
RSIPO17	83	25-3	ISIPO17	98	21-6	DONE	27	7-5
RSIPO18	84	23-2	ISIPO18	97	21-2	PE	34	7-7
RSIPO19	85	23-4	ISIPO19	96	21-7	WDE	1	7-0
RSIPO20	86	25-6	ISIPO20	95	21-3			
RSIPO21	87	23-0	ISIPO21	94	21-1			
RSIPO22	88	23-5	ISIPO22	93	21-0			
RSIPO23	89	23-3	ISIPO23	92	23-6			
RSIPO24	90	23-7	ISIPO24	91	21-4			

Note: The data from the output data memory address lines (pins 14 through 25) were not sensed due to the limited supply of acquisition probes.

To get the logical zero input to the DUT to be the same as the chip ground, the probes' 5.2V differential had to come from a separate 5.2V power supply biased by -0.7V giving the probe input differential of 4.5V to -0.7V with the probe output realizing a differential of 3.8V to 0V. Figure 2-1 shows the biasing scheme used.

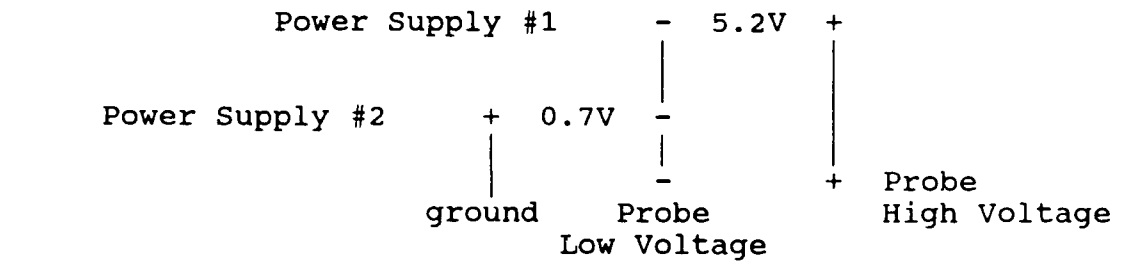


Figure 2.1: Probe Voltage Biasing Scheme.

2.3.2.3 Clocking Considerations. During testing four different clocks were used by the test equipment and chip, two test system clocks and four chip clocks.

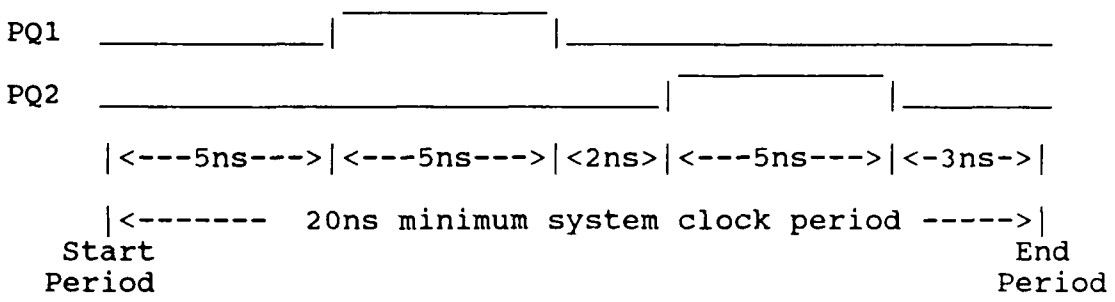
The main system clock was programmed using the DAS 9200's Run Control Menu of the Device Verification Application. This clock could only be set to preprogrammed frequencies, 50MHz maximum to 1kHz minimum, and was used to determine the over all period of all clock cycles. The other system clock was a 50% duty cycle clock that triggered the acquisition probes half way through the system clock's period to sense the data comming from the chip.

The four chip clocks were the two PQ1 and the two PQ2

clocks. Each of the two main WFTA16 sections, control and arithmetic sections, had independent clocks. These clocks were generated by special strobe lines associated with data stimulus probe pods. These lines could be programmed within the Channel Allocation Menu of the Device Verification Application. The programmable parameters were the pulse width, 5ns minimum to 80ns maximum, and pulse delay from the start of the system clock period, 5ns minimum to 95ns maximum.

Each of the four chip clocks were programmed to operate during the same clock cycle such that the PQ1 clocks pulsed together as did the PQ2 clocks. The PQ1 and PQ2 clocks were also programmed to pulse such that they did not overlap, thus avoiding race conditions caused by both clocks being high. With the predetermined selection of pulse widths, delays, and system clock periods, the actual clock frequencies during test had to be simulated when maximum circuit frequencies were being done. As an example, 70MHz was found to be the maximum operating frequency of any portion of the WFTA16. To simulate this, both PQ1 and PQ2 signals were set to the minimum pulse width of 5ns, PQ1 was brought high first and PQ2 was brought high 7ns later. This gave a 2ns null between the fall of PQ1 and the rise of PQ2. Due to test system limitations, the minimum time from the fall of PQ2 to the rise the next PQ1 was 8ns for a total 20ns period; but since no processing occurs between the fall of PQ2 and the next rise of PQ1, a uniform

null of 2 ns could be assumed which would yield a 14ns period or 70MHz operations.



Similar schemes were used to determine the maximum operating frequencies of circuit sections that did not acheive the 70MHz goal.

2.3.3 Test Data.

2.3.3.1 Trivial Transform Attempts. To see if the WFTA16 chip was functioning entirely as planned, trivial or DC transforms were attempted using chips T and U. Each of these attempts consisted of inputing 16 identical data words over the required 32 clock cycles required to load the PISO registers then reading the 16 output data words from the SIPO registers. In each case, the expected output was one word identical to the input words followed by 15 words representing zeros.

Due to designed timing delays while the WFTA16 chip initializes itself, the first data word was not read into the PISO registers until six clock cycles from the time the OPR signal goes high. Then 108 clock cycles later, 114 clock

cycles after OPR, the first output word was ready to be read from the SIPO registers. Each output word was valid for two clock cycles with the first word being the Fourier transform DC value and the following words being the frequency terms.

To initialize the WFTA16 prior to a transform six bits of information must be loaded onto the chip in a specific order. First the three scale factor bits must be loaded, then the two DFT size bits and the watchdog control bit must be loaded. The scale factor bits are loaded when the OPR command is low and the LD command is high, while the size and watchdog bits are loaded when both OPR and LD are low. The following routine was used each time a trivial transform was attempted:

```
Clock Cycle 0 through 4 - Load = 1
                          OPR  = 0
                          SF3, SF2, SF1 = 000

Clock Cycle 5 through 9 - Load = 0
                          OPR  = 0
                          SF3, SF2, SF1 = 000

Clock Cycle 10 to end   - Load = 0
                          OPR  = 1
                          SF3, SF2, SF1 = 000
```

This routine loaded a scale factor of zero into the scale factor flip-flops, a DFT size of 4080-points into the DFT size flip-flops, and set the watchdog error detection circuit off before beginning the transform operation. The first valid input data words were sensed beginning in clock cycle 16, while the ouput first became valid on clock cycle 124 then were expected to repeat itself every 32 clock cycles.

To facilitate the handling of output data, the DAS 9200 was programmed to display the 24 output bits from each of the SIPO registers in decending order from the MSB to the LSB, with the MSB actually being the parity bit as it is with the input data. Also this test was run using a 200ns clock period.

Initial Attempts. In no case were any of the initial trivial transforms successful. The data received should have been consistant from one 32 period data cycle to another, but was not. Also, each chip yielded different results each time a test was run and no two chips showed the same results.

The most important result from above is implied by the fact that the two chips gave different outputs for the same inputs. This indicates that each chip has a different logic implementation. These differences could be caused by the existance of the numerous design rule errors as shown in table 1.1. These design rules errors, when combined with the inherent variations of the fabrication process, may have caused variation among the separate WFTA16 dies.

Further testing was required in an attempt to isolate errors and to determine the actual cause of those errors. The testing that followed was broken out into functional areas using the test structure designed by Shephard.

Later Testing. After the pad test functional test, discussed in section 2.3.3.3, identified chips #3 oxide, E,

and G as potentially error free, trivial transforms were attempted again. Using those three chips, a transform using a DC value of zero was attempted. During earlier testing on different chips this test always met with total failure.

To perform this test, the two chip clocks were programmed to have 10ns pulse widths with the rise of PQ1 60ns before the fall of PQ2. The system was programmed to operate at 5 MHz. Various chip voltages were tried in attempts to generate a sucessful transform.

Using both trivial and non-trivial transforms, chip E showed consistant and repeatable results. When a DC value of zero was input, all output words were also zero and the parity bit was set to one. For the non-trivial transforms, the sixteen most significant bits were shifted down one position toward the LSBs, the seven LSBs did not closely resemble the expected data, and the parity bit always reflected the correct parity.

Chip G showed the same results with the exception of a stuck-at-fault showing at the RSIPO04 output.

The #3 oxide chip did not yield results that reflected expected data.

2.3.3.2 XROM Input Address Observations. During the initial attempts at performing trivial transformations, the input memory address lines, IA1 through IA12, were observed to be changing state. When compared to the data

gathered through circuit simulation as well as the data used to automatically generate the layout of the address generation circuitry, no errors were found.

To acquire the address data, the DAS 9200 was programmed to sense the address pins after the fall of PQ2 and before the next rise of PQ1.

Though the address generation circuit control signals were not directly observable, the address generation circuit, a customized AFIT XROM, was shown to operate sucessfully at a maximum frequency of 70 MHz. This was observed, using multiple chips and simulating a 70 MHz clock frequency, through the primary outputs of the input memory address pins.

2.3.3.3 Input/output Pad Test. The simplest functional test to run was the input/output pad test. This test takes inputs from the RPISO07 through RPISO24 and IPISO07 through IPISO24 pins and routs them through single inverters to the RSIPO07 through RSIPO24 and ISIPO07 through ISIPO24 output pads. The six LSB's of each SIPO register's output pads are reserved for the control signals generated by the arithmetic control section which is discussed in section 2.3.3.4.

To initialize the WFTA16 prior to a pad test four bits of information must be loaded into the chip's test PLA. This is accomplished by setting the four LSB's of the RPISO input word to a hexadecimal 7. The following routine was used to initialize the WFTA16 chip and test PLA each time a pad test

was run:

Clock Cycle 0 through 4 -	Load = 1	RPISO04 = 0
	Test = 0	RPISO03 = 1
	OPR = 0	RPISO02 = 1
		RPISO01 = 1
Clock Cycle 5 through 9 -	Load = 1	RPISO04 = 0
	Test = 1	RPISO03 = 1
	OPR = 0	RPISO02 = 1
		RPISO01 = 1
Clock Cycle 10 to end -	Load = 0	RPISO04 = 0
	Test = 1	RPISO03 = 1
	OPR = 0	RPISO02 = 1
		RPISO01 = 1

To facilitate the handling of output data, the DAS 9200 was programmed to display the 18 MSB's from each of the SIPO output pads in decending order from RSIPO24 to RSIPO07 and ISIPO24 to ISIPO07.

Since the test structure was not designed to operate at extremely high frequencies, this test was run at 1 MHz. It was found that by setting the chip power or Vdd pins to 5.2V gave the most consistant and repeatable results.

All 16 chips making it past the DC test phase were tested using the test vectors listed in table 2.4 and gave the results shown in table 2.5.

The faults as shown in table 2.5 do not necessarily mean the output pads are bad. What they mean is that the noticed faults occur either at the input pads, within the test bus or controlling t-gates and inverters, or at the output pads. Probing of the circuit is required to isolate the faults.

Table 2.4 Pad Test Input Vectors and Expected Results.

Input Vectors		Expected Outputs	
RPISO	IPISO	RSIPO	ISIPO
777777	777777	000000	000000
777777	777777	000000	000000
525252	525252	252525	252525
525252	525252	252525	252525
252525	252525	525252	525252
252525	252525	525252	525252
000000	000000	777777	777777
000000	000000	777777	777777

Note: Data is presented in octal format and applies to the PISO and SIPO pads 24 down to 7.

2.3.3.4 Control Section. The control section consists of two related, but separate, control signal generation logic circuits. One circuit generates the control signals for the memory read/write address XROM circuit, while the other set of logic generates all control signals required to process the input data through the registers and arithmetic sections.

The XROM control signals were shown to be working correctly through the direct observations of the XROM output as explained in section 2.3.3.2.

The control signals required for register operations were all output directly to the six least significant ouput pads of each of the SIPO pad banks. These signals are available directly during all tests except those tests in which the output of the SIPO registers are required. All observed signals were changing state correctly when chips T and U were

Table 2.5: Pad Test Results.

Chip	Indicated Faults Appearing at Outputs		Chip	Indicated Faults Appearing at Outputs	
#3 Oxide	None		GND-1	IPISO07	short
				IPISO08	short
E	None			IPISO09	short
				IPISO10	short
F	None			IPISO13	short
				IPISO14	short
GND-4	RSIPO24	s-a-1			
	ISIPO23	s-a-0	I	RSIPO24	s-a-1
	ISIPO14	s-a-0		ISIPO23	s-a-0
	ISIPO12	s-a-1		ISIPO19	s-a-0
	ISIPO09	s-a-0		ISIPO12	short
				ISIPO09	s-a-0
GND-2	All bits	s-a-0			
			Y	RSIPO24	s-a-1
U	RSIPO23	short			
	ISIPO12	s-a-0	S	ISIPO23	s-a-0
	ISIPO09	s-a-0		ISIPO17	s-a-0
T	ISIPO23	s-a-0	#1 oxide	RSIPO24	s-a-1
				RSIPO22	s-a-1
C	ISIPO23	s-a-0		ISIPO24	s-a-1
				ISIPO22	s-a-0
H	ISIPO23	s-a-0		ISIPO20	s-a-0
				ISIPO19	s-a-0
#2 oxide	ISIPO23	s-a-0		ISIPO17	s-a-0
	ISIPO09	s-a-0		ISIPO12	short
				ISIPO09	s-a-0
D	ISIPO07	s-a-0			

Note: s-a-1 represents a stuck at one fault.
s-a-1 represents a stuck at zero fault.
short represents two or more data paths shorted together.

operating after a scale factor of zero was loaded. Only the four scale factor dependent signals; zerofill, shift right PISO (SRpiso), parity check (parchk), and parity latch (par-latch); did not operate correctly when the scale factor was

changed to one through seven. In every case, these four signals continued to change state as if the scale factor were zero. This is probably due to a logic error in generating the set and reset signals required for their SR flip-flcps. The observed timing of these signals is presented in table 2.6. An explaination of all WFTA16 control signal names are included in appendix A.

Table 2.6: Observed Arithmetic and Register Control Signals through one 32 clock cycle block for Test Chips T and U.

Output Pad	Signal Name	Logical Sequence
ISIPO05	SDpiso	01010101010101010101010101010101010101
ISIPO04	SRpiso	01111111111111111111111111111111111111
ISIPO06	Lpiso	10000000000000000000000000000000000000
ISIPO02	zerofill	01000000006000000000000000000000000000
ISIPO03	parchk	01111111111111111111111110000000000000
ISIPO01	par-latch	00000000000000000000000010000000000000
RSIPO05	rcalc	11111111111100000000000000011111111111
RSIPO04	par-append	00000000000001000000000000000000000000
RSIPO03	Lsipo	00000000000000100000000000000000000000
RSIPO02	SDsipo	01010101010101010101010101010101010101
RSIPO06	mult-rnd	00000010000000000000000000000000000000

Two signals are required for arithmetic control, the reset adders and multiplier round signals. The multipler round signal was directly observable through an output pin and was changing state correctly. The reset adders signal was not directly observable but it was tested for during arithmetic section tests.

The only other control signal directly observable was the

reset scaling (rst-scal) control bit. This bit was set high two clock cycles after the operate command was raised, then returned low 106 cycles later when the first set of output data was ready. This timing was what was expected.

2.3.3.5 PISO Register. These registers were tested by inputing predefined bit patterns then sensing the register output after the parity checking and zerofill circuitry. Twenty-four bit words were input in parallel, while 32 bit words were output serially. The registers sucessfully shifted the parallel data into the register, latched it over to the serial side of the register, and added a zero bit as the data's LSB before outputing the serial words. To extend the data to the required 32 bits for serial processing, eight bits of sign extensions were required, but in no case did this happen when the MSB was a one. In every case the eight MSB's of every data word were zeros. This is probably due to a feedback error within the speciallized PISO cell that should form the sign extensions. Using the test bus output from the PISO register, a maximum operating frequency of 30 MHz was found. This frequency is, in all likelihood, slower than the true maximum operating frequency as the output inverters from the register were not designed to drive long transmission lines terminating at the output pads.

2.3.3.6 Preadder Subsection. This section was tested only for signal path continuity and functionality based on changing one input signal at a time. This was accomplished by inputing a bit stream into one of the sixteen preadder inputs at a time and checking to see if the expected outputs change. Then all inputs were set to the same value and the results were checked.

To initialize the WFTA16 prior to a preadder test four bits of information must be loaded into the chip's test PLA. This is accomplished by setting the four LSB's of the RPISO input word to a hexadecimal four. The following routine was used to initialize the WFTA16 chip and test PLA each time a preadder test was run:

Clock Cycle 0 through 4 -	Load = 1	RPISO04 = 0
	Test = 0	RPISO03 = 1
	OPR = 0	RPISO02 = 0
		RPISO01 = 0
Clock Cycle 5 through 9 -	Load = 1	RPISO04 = 0
	Test = 1	RPISO03 = 1
	OPR = 0	RPISO02 = 0
		RPISO01 = 0
Clock Cycle 10 to end -	Load = 0	RPISO04 = 0
	Test = 1	RPISO03 = 1
	OPR = 1	RPISO02 = 0
		RPISO01 = 0

To facilitate the handling of output data, the DAS 9200 was programmed to display the 18 preadder results from each of the preadder sections from each of the SIPO output pads in decending order from RSIPO22 to RSIPO07 and ISIPO22 to ISIPO07.

The expected results from this test were drawn from table 2.7. For example, if all inputs were held at zero except h8, then the output r101 at RSIPO24 should be the two's complement of h8 after three clock cycles, while the r201 result at RSIPO21 should equal h8 after three clock cycles.

Table 2.7: Preadder test data output pad assignment list and relationships to input data.

Output Pad	Preadder Result Label	Relationship to Inputs [Taylor]
RSIPO24	r101	= h0 - h8
RSIPO17	r109	= h4 - h12
RSIPO21	r201	= h0 - h4 + h8 - h12
RSIPO18	r203	= -h2 + h6 - h10 + h14
RSIPO08	r208	= h1 + h7 - h9 - h15
RSIPO13	r209	= h1 - h7 - h9 + h15
RSIPO07	r210	= h3 + h5 - h11 - h13
RSIPO12	r211	= -h3 + h5 + h11 - h13
RSIPO10	r212	= h2 + h6 - h10 - h14
RSIPO15	r213	= h2 - h6 - h10 + h14
RSIPO22	r300	= h0 + h2 + h4 + h6 + h8 + h10 + h12 + h14
RSIPO20	r301	= h0 - h2 + h4 - h6 + h8 - h10 + h12 - h14
RSIPO23	r302	= h1 + h3 + h5 + h7 + h9 + h11 + h13 + h15
RSIPO19	r303	= -h1 + h3 - h5 + h7 - h9 + h11 - h13 + h15
RSIPO11	r304	= h1 + h3 - h5 - h7 + h9 + h11 - h13 - h15
RSIPO16	r305	= h1 - h3 - h5 + h7 + h9 - h11 - h13 + h15
RSIPO14	r306	= h1 - h3 + h5 + h7 - h9 + h11 - h13 - h15
RSIPO09	r307	= h1 + h3 + h5 + h7 - h9 - h11 - h13 - h15

As can be seen in table 2.7, if all 16 preadder inputs are assigned the same value, then all results should be zero except for r300 and r302 which should have values equal to eight times the input. These two results are later added together in the postadder section to yield the DC term of the

Fourier transform.

The information listed in table 2.7 reflects only the testing of the real preadder section. The imaginary section mirrors the real section exactly with the outputs going to the ISIPO pads and the inputs comming from the IPISO pads. Both preadder sections were tested at the same time as they are both physically and logically isolated.

Table 2.8 shows the relationship of the required data to input pad and expected outputs. This table reflects the real preadder only, but again the two preadder sections mirror each other and the imaginary inputs and outputs are assigned to the IPISO and ISIPO pads.

Table 2.8: List of preadder inputs and their expected dependent output signals.

Input Pad	Preadder Data Label	Expected Dependent Outputs [Taylor]
RPISO07	h0	==> r101, r201, r300, r302
RPISO08	h1	==> r208, r209, r302, r303, r304, r305, r306, r307
RPISO09	h2	==> r203, r212, r213, r300, r301
RPISO10	h3	==> r210, r211, r302, r303, r304, r305, r306, r307
RPISO11	h4	==> r109, r201, r300, r301
RPISO12	h5	==> r210, r211, r302, r303, r304, r305, r306, r307
RPISO13	h6	==> r203, r212, r213, r300, r301
RPISO14	h7	==> r208, r209, r302, r303, r304, r305, r306, r307
RPISO15	h8	==> r101, r201, r300, r301
RPISO16	h9	==> r208, r209, r302, r303, r304, r305, r306, r307
RPISO17	h10	==> r203, r212, r213, r300, r301
RPISO18	h11	==> r210, r211, r302, r303, r304, r305, r306, r307
RPISO19	h12	==> r109, r201, r300, r301
RPISO20	h13	==> r210, r211, r302, r303, r304, r305, r306, r307
RPISO21	h14	==> r203, r212, r213, r300, r301
RPISO22	h15	==> r208, r209, r302, r303, r304, r305, r306, r307

The results of this test using chips C and D showed there is functionality between the inputs and the outputs.

2.3.3.7 Multiplier Subsection Test. This section was not tested as a part of this thesis effort due to time limitations, but signal path continuity and simple functionality can be tested for by injecting bit streams into each of the 18 bit-serial multiplier rows of each of the multipler sections. Table 2.9 shows the relationship of the real inputs to the outputs through the multiplier rows. Again, since the real and imaginary sections are exact mirrors of each other, the imaginary relationships are the same as the reals.

Table 2.9: Multiplier input through output relationships.

Input Pad	Preadder Label	Multiplier Value [Taylor]	Multiplier Label	Output Pad
RPISO07	r210	-1.30656296487638	t17	RSIPO07
RPISO08	r208	0.54119610014619	t16	RSIPO08
RPISO09	r307	-0.92387953251128	t15	RSIPO09
RPISO10	r212	-0.70710678118654	t14	RSIPO10
RPISO11	r304	-0.70710678118654	t13	RSIPO11
RPISO12	r211	0.00000000000000	t12	RSIPO12
RPISO13	r209	1.00000000000000	t11	RSIPO13
RPISO14	r306	1.00000000000000	t10	RSIPO14
RPISO15	r213	-0.54119610014619	t9	RSIPO15
RPISO16	r305	1.30656296487638	t8	RSIPO16
RPISO17	r109	0.38268343236510	t7	RSIPO17
RPISO18	r203	0.70710678118654	t6	RSIPO18
RPISO19	r303	0.70710678118654	t5	RSIPO19
RPISO20	r301	1.00000000000000	t4	RSIPO20
RPISO21	r201	1.00000000000000	t3	RSIPO21
RPISO22	r300	1.00000000000000	t2	RSIPO22
RPISO23	r302	1.00000000000000	t1	RSIPO23
RPISO24	r101	1.00000000000000	t0	RSIPO24

To initialize the WFTA16 prior to a multiplier test four bits of information must be loaded into the chip's test PLA. This is accomplished by setting the four LSB's of the RPISO input word to a hexadecimal A. The following routine is required to initialize the WFTA16 chip and test PLA each time a multiplier test is run:

Clock Cycle 0 through 4 -	Load = 1	RPISO04 = 1
	Test = 0	RPISO03 = 0
	OPR = 0	RPISO02 = 1
		RPISO01 = 0
Clock Cycle 5 through 9 -	Load = 1	RPISO04 = 1
	Test = 1	RPISO03 = 0
	OPR = 0	RPISO02 = 1
		RPISO01 = 0
Clock Cycle 10 to end -	Load = 0	RPISO04 = 1
	Test = 1	RPISO03 = 0
	OPR = 1	RPISO02 = 1
		RPISO01 = 0

2.3.3.8 Postadd Section Test. This section was not tested as a part of this thesis effort due to time limitations, but signal path continuity and simple functionality can be tested for by injecting bit streams into each of the 18 real and imaginary postadder input lines. Tables 2.10 and 2.11 show the relationship of the real inputs to the outputs through the postadder. If the data input through the IPISO pads is the same as the corresponding RPISO pads then the expected outputs for both sides would be the same.

Table 2.10: Postadder test data output pad assignment list and relationships to input data.

Input Pad	Output Label		Output Relationship to Inputs [Taylor]
RSIPO07	h0	=	t0 + t1
RSIPO08	h1	=	t4 + t6 - t7 + t8 - u12 u14 - u15 - u16
RSIPO09	h2	=	t3 + t5 - u11 - u13
RSIPO10	h3	=	t4 - t6 + t7 - t9 + u12 - u14 - u15 + u17
RSIPO11	h4	=	t2 - u10
RSIPO12	h5	=	t4 - t6 - t7 + t9 - u12 + u14 - u15 + u17
RSIPO13	h6	=	t3 - t5 + u11 - u13
RSIPO14	h7	=	t4 + t6 + t7 - t8 + u12 + u14 - u15 - u16
RSIPO15	h8	=	t0 - t1
RSIPO16	h9	=	t4 + t6 + t7 - t8 - u12 - u14 + u15 + u16
RSIPO17	h10	=	t3 - t5 - u11 + u13
RSIPO18	h11	=	t4 - t6 - t7 + t9 + u12 - u14 + u15 - u17
RSIPO19	h12	=	t2 - u10
RSIPO20	h13	=	t4 - t6 + t7 - t9 - u12 + u14 + u15 - u17
RSIPO21	h14	=	t3 + t5 + u11 + u13
RSIPO22	h15	=	t4 + t6 - t7 + t8 + u12 + u14 + u15 + u16

Note: The inputs prefaced with a 't' are from the real multiplier and the inputs prefaced with a 'u' are from the imaginary multiplier.

To initialize the WFTA16 prior to a postadder test four bits of information must be loaded into the chip's test PLA. This is accomplished by setting the four LSB's of the RPISO input word to a hexadecimal six. The following routine is required to initialize the WFTA16 chip and test PLA each time a preadder test is run:

Clock Cycle 0 through 4 -	Load = 1	RPISO04 = 0
	Test = 0	RPISO03 = 1
	OPR = 0	RPISO02 = 1
		RPISO01 = 0
Clock Cycle 5 through 9 -	Load = 1	RPISO04 = 0
	Test = 1	RPISO03 = 1
	OPR = 0	RPISO02 = 1
		RPISO01 = 0

Table 2.11: List of postadder inputs and their expected dependent output signals.

Input Pad	Preadder Data Label		Expected Dependent Output Labels [Taylor]
RPISO07	t0 ==>	real	h0, h8
RPISO08	t1 ==>	real	h0, h8
RPISO09	t2 ==>	real	h4, h12
RPISO10	t3 ==>	real	h2, h6, h10, h14
RPISO11	t4 ==>	real	h1, h3, h5, h7, h9, h11, h13, h15
RPISO12	t5 ==>	real	h2, h6, h10, h14
RPISO13	t6 ==>	real	h1, h3, h5, h7, h9, h11, h13, h15
RPISO14	t7 ==>	real	h1, h3, h5, h7, h9, h11, h13, h15
RPISO15	t8 ==>	real	h1, h7, h9, h15
RPISO16	t9 ==>	real	h3, h5, h11, h13
RPISO17	t10 ==>	imag	h4, h12
RPISO18	t11 ==>	imag	h2, h6, h10, h14
RPISO19	t12 ==>	imag	h1, h3, h5, h7, h9, h11, h13, h15
RPISO20	t13 ==>	imag	h2, h6, h10, h14
RPISO21	t14 ==>	imag	h1, h3, h5, h7, h9, h11, h13, h15
RPISO22	t15 ==>	imag	h1, h3, h5, h7, h9, h11, h13, h15
RPISO23	t16 ==>	imag	h1, h7, h9, h15
RPISO24	t17 ==>	imag	h3, h5, h11, h13

Clock Cycle 10 to end - Load = 0 RPISO04 = 0
Test = 1 RPISO03 = 1
OPR = 1 RPISO02 = 1
RPISO01 = 0

2.3.3.9 SIPO Register Test. This test was not run as a part of this thesis effort due to time limitations, but these registers can be tested by inputing predefined bit patterns then sensing the register output after the parity checking and zerofill circuitry. Sixteen 32-bit long words are serially shifted into each of the SIPO registers from the RPISO07 through RPISO22 and IPISO07 through IPISO22 pads. Then 16 24-bit words are shifted out of the SIPO registers in

parallel throught the SIPO pads.

To initialize the WFTA16 prior to a sipo register test four bits of information must be loaded into the chip's test PLA. This is accomplished by setting the four LSB's of the RPISO input word to a hexadecimal one. The following routine is required to initialize the WFTA16 chip and test PLA each time a sipo register test is run:

Clock Cycle 0 through 4 -	Load = 1	RPISO04 = 0
	Test = 0	RPISO03 = 0
	OPR = 0	RPISO02 = 0
		RPISO01 = 1
Clock Cycle 5 through 9 -	Load = 1	RPISO04 = 0
	Test = 1	RPISO03 = 0
	OPR = 0	RPISO02 = 0
		RPISO01 = 1
Clock Cycle 10 to end -	Load = 0	RPISO04 = 0
	Test = 1	RPISO03 = 0
	OPR = 1	RPISO02 = 0
		RPISO01 = 1

2.3.3.10 Other Functional Tests. Using the built in WFT16 test structure it is possible to test the above functional areas in groups. For the functional test groups, the Shephard thesis must be consulted.

3. Cell Library Improvements

3.1 Introduction

As seen in table 1.1, the WFTA arithmetic and register subcells do not meet current MOSIS fabrication design rules. In order to assure compatability with those rules, each of the cells listed in table 1.1 needed to be redesigned. In many cases, these redesigned cells could not retain the same interface with their neighbor cells, so the neighbor cells also had to be redesigned.

During the redesign process, a high degree of attention was placed on making the cells with as little cell boundry overlapping as possible. This resulted in complete groups of cells being able to be laid out without having to expand the cells to ensure correct placement. This also helped greatly when laying out large arrays of similar cells.

Another strong design criteria used was to foresee the required global routing of power, ground, clocks, control, and data signals and to incorporate this routing into existing cells. This resulted in macrocells that ended up being self routing. The previous WFTA cells required that macrocells be laid out and the global routing be accomplished before expanding individual subcells to accomplish the final wiring.

Cell sizes were also taken into consideration. Since one of the goals of the WFTA project is to integrate an entire 4080-point processor onto a single wafer [Linderman], it is

necessary that each cell be as small as possible, as well as function correctly. Even with this in mind, some cells were not minimized in order to preserve their compatability with neighbor cells.

Finally, reliability was taken into consideration. Without increasing subcell areas, metal lines carrying data and control signals were routed straight through each subcell instead of going through multiple corners. Also each of those metal lines was expanded to four lambda wide from the three lambda used in the previous cells; again this was done without increasing cell areas. Power and ground lines were also routed straight and expanded. Additional power and ground lines were placed within the cells as space allowed to better distribute current loads. Also metal to diffusion contacts and metal to metal vias were doubled in size as space allowed to lower potential current densities passing from one layer to another.

In all cases, the redesigned cells were simulated side-by-side using a switch level, event driven simulator on AFIT's Galaxy computer. In all cases, the simulation results were identical.

Also during the redesign process, the cell library was reorganized to better reflect subcell functionality and physical groupings.

3.2 Basic Cell Redesign

3.2.1 Parallel in Serial out Register Cells. The parallel in serial out (PISO) cells were designed to join together to accept parallel data input words and store them until the parallel side of the register is full, then transfer the data to the serial side and serially shift the data out to the arithmetic circuitry. When put together, the register does more than hold data, it also uses the parzer-mine cell to modify data with leading zeros and to check the parity of the input data. Sign extensions are automatically generated by the special piso cell at the most significant bit end of a data word.

As a result of the redesign of these cells, all design rule errors were eliminated and, as table 3.1 shows, cell areas were diminished in all cases except two, but those two cells include the automatic global routing the replaced cells don't have. Also, the number of cells required for a total PISO register was decreased from seven to five.

Individual explanations of cell functions and interfaces are included in appendix B.

3.2.2 Adder/subtractor Cells. The adder/subtractor (addsub) cells were designed to automatically rout all signals common to all cells. This resulted in no hand wiring of a bank of addsub cells when extra wiring was required to correctly interface the previous addsub delay cells to the

Table 3.1: PISO Register Cell Comparison.

Redesigned Cell Name	Dimensions (lambda)	Replaced Cell Name	Dimensions (lambda)	Area Change
piso-mine-msb	72 x 104	piso_cell_L	77 x 120	-19%
piso-mine	72 x 104	piso_cell	77 x 117	-17%
		piso_cell_R	77 x 125	-22%
piso-mine-inv[1]	164 x 208	piso_inv	96 x 117	52%
		piso_inv_L	77 x 120	85%
parzer-mine	72 x 205	parzer_cell	74 x 232	-14%
parzer-mine -inv[2]	164 x 205	parzer_inv	96 x 236	48%

1: This cell replaces two cells and performs the same function as those cells in addition to the automatic routing of power, ground, clock, control, and data signals.

2: This cell performs the same function as the replaced cell in addition to the automatic routing of power, ground, clock, control, and data signals.

rest of the addsub bank.

As a result of redesign, all design rule errors were eliminated, as table 3.2 shows, no savings in number of required cells was realized.

Individual explanations of cell functions and interfaces are included in appendix B.

3.2.3 Multiplier Cells. Each of the five redesigned multiplication cells were designed to be as modular and regular as possible. Each of the cells has the same bank of four master slave flip-flops to isolate the two carry and the

Table 3.2: Adder/Subtractor Cell Area Comparison.

Redesigned Cell Name	Dimensions (lambda)	Replaced Cell Name	Dimensions (lambda)	Area Change
addsub-mine	132 x 219	addsubmod	132 x 222	- 1%
addsub-mine -delay	44 x 219	addmsff[2]	39 x 133	86%
addsub-mine -end-cap[1]	93 x 219	addcon	83 x 222	10%
addsub-mine -inv[1]	126 x 219	add_inv	79 x 222	57%

1: This cell performs the same function as the replaced cell in addition to the automatic routing of power, ground, clock, control, and data signals.

2: This cell required additional routing to make it compatable with the addsubmod cell. The redesigned cell automatically incorporates that routing.

two data bits generated by the cell. Each cell has the same adder circuitry. And the triple master slave flip-flop at the input end of each cell is identical with minor adjustments based on the multiplication size and positive or negative.

As a result of the redesign of these cells, all design rule errors were eliminated and the cell area was diminished or unchanged in all cases except two, but those two cells include the automatic global routing the replaced cells don't have. Also, as table 3.3 shows, the number of cells required for a complete multiplier array was decreased from seventeen to seven.

Table 3.3: Multiplier Cell Area Comparison.

Redesigned Cell Name	Dimensions (lambda)	Replaced Cell Name	Dimensions (lambda)	Area Change
mult-mine -0plus	87 x 297	Rmult0a	87 x 429	-31%
		Rmult0	87 x 429	-31%
		mult0a	87 x 297	0%
		mult0	87 x 297	0%
		Lmult0a	87 x 402	-26%
		Lmult0	87 x 402	-26%
mult-mine -1plus	87 x 297	Rmultp1a	87 x 429	-31%
		multp1a	87 x 297	0%
		Lmultp1a	87 x 402	-26%
mult-mine -1minus	87 x 297	Rmultn1a	87 x 429	-31%
		multn1a	87 x 297	0%
		Lmultn1a	87 x 402	-26%
mult-mine -2plus	87 x 297	multp2a	87 x 297	0%
mult-mine -2minus	87 x 297	multn2a	87 x 297	0%
mult-mine -end-cap[1]	87 x 297	multcon	80 x 297	9%
		rmultcon	80 x 297	9%
mult-mine -inv[1]	106 x 297	mult_inv	104 x 297	2%

1: This cell performs the same function as the replaced cell in addition to the automatic routing of power, ground, clock, control, and data signals.

Individual explanations of cell functions and interfaces are included in appendix B.

3.2.4 Serial in Parallel out Register Cells The serial in parallel out (SIPO) cells were designed to join together to accept serial data input words and store them until the serial side of the register is full, then transfer the data to the

parallel side and shift the data out to the output pads. When put together, the register does more than hold data, it also uses the parrnd cell to modify data by calculating the parity of data as it comes from the arithmetic section and appending the correct parity bit to the data in the register to ensure all output data has odd parity. The parrnd cell also rounds the arithmetic data to 23 bits as it loads the SIPO register cells.

As a result of the redesign of these cells, all design rule errors were eliminated and, as shown in table 3.4, cell

Table 3.4: SIPO Register Cell Area Comparison.

Redesigned Cell Name	Dimensions (lambda)	Replaced Cell Name	Dimensions (lambda)	Area Change
parrnd-mine	72 x 263	parrnd_cell	81 x 367	-36%
parrnd-mine-inv[2]	116 x 263	parrnd_inv	80 x 356	7%
sipo-mine	72 x 104	sipo_cell	81 x 125	-26%
		sipo_cell_MSB	81 x 135	-32%
sipo-mine-out	72 x 104	sipo_cell_D	81 x 125	-26%
		sipo_cell_DMSB	81 x 135	-32%
sipo-mine-inv[1]	164 x 208	sipo_inv	96 x 125	42%

1: This cell replaces two cells and performs the same function as those cells in addition to the automatic routing of power, ground, clock, control, and data signals.

2: This cell performs the same function as the replaced cell in addition to the automatic routing of power, ground, clock, control, and data signals.

areas were diminished in all cases except two, but those two cells include the automatic global routing the replaced cells don't have. Also, the number of cells required for a total SIPO register was decreased from seven to five.

Individual explanations of cell functions and interfaces are included in appendix B.

3.3 WFTA16 Macrocell Designs

After each set of redesigned cells were finished, they were laid out to form WFTA16 subsections. Each of the two major register sections and the three arithmetic sections were laid out. As table 3.5 shows, only the preadder and multiplier arrays showed an increase in area over the previous sections. These slight increases in area are as a direct result of the inclusion of global routing within subcells where the global routing didn't exist in the previous cells.

Table 3.5: WFTA16 Functional Area Comparison.

Functional Area	Dimensions (lamba) Redesigned	Existing	Area Change
PISO Register	1152 x 2496	1191 x 2827	-15%
Preadder Array	1451 x 929	1670 x 783	2%
Multiplier Array	1800 x 3876	1573 x 4098	8%
Postadder Array	1319 x 857	1584 x 905	-21%
SIPO Register	1152 x 2496	1236 x 3010	-23%

3.4 Cell Library Organization

3.4.1 Initial Organization. There were in excess of 200 basic design cells associated with the basic WFTA cell library prior to this thesis. By functional area, the number of basic cells were as follows:

Register cells	
SIPO	9
PISO	9
Arithmetic Cells	
Adder/subtractors	6
Multipliers	17
Control	71
Test	7
XROM	70
Pads	16
	205

The WFTA cell library set up on the AFIT Galaxy computer consisted of an overall wfta directory with five subdirectorys and one parallel directory.

The wfta subdirectories and the types of wfta cells they contain were as follows:

arith - PISO register cells, SIPO register cells, parzer cells, parrnd cells, Parity checking cells, Adder/subtractor cells, Multiplier cells, Clock inverter cells, Arithmetic control cells

control - Ring counter cells, Assorted PLA subcells, Flip-flops, Clock inverter cells

pla - Assorted PLA cells, Test cells

xrom - All cells required to generate an xrom

x_addr_gen - All cells required to generate an xrom controller

The one parallel directory was the vhsicpad directory.

This directory contained all input, output, clock, power, and ground pads used to layout a WFTA chip. Some of these pad files were modified specifically for use with the WFTA project.

3.4.2 Functional Reorganization.

As work progressed and cells were redesigned, the following directory structure was generated to better reflect cell functionality and physical groupings within an actual WFT processor:

registers - all SIPO and PISO register cells as well as their associated clock inverters and local control cells.

arith - all adder/subtractor, adder, subtractor, and multiplier cells as well as their associated clock inverters and local control cells.

control - all ring counter, PLA, flip-flop, and test specific cells as well as their associated clock inverters and local control cells.

xrom - all cells required to generate an xrom and its controlling address generator cell.

pads - all WFTA specific input, output, clock, power and ground pads required for a WFTA chip.

4. Cell Library Verification

4.1 Introduction

To verify that each of the basic cells would work correctly when fabricated, a series of test chips were designed. These test chips were designed to be submitted to MOSIS as 40 pin tiny chips with 2 micron feature sizes. Tiny chips are smaller than full sized chips and are fabricated through MOSIS on a space available basis. Tiny chips are normally used to charactorize subcircuits prior to full scale fabrication.

The tiny chips were designed to output as many primary output signals to output pads as possible. Probe pads were also placed within the chips, along data lines, to allow for sensing intermediate results.

4.2 Test Chips

In order to check the operations of each of the redesigned cell when fabricated, five tiny chips were designed. Each chip was designed to test a functional area.

All chips were designed for standard MOSIS 2-micron, 40-pad, tiny chip fabrication. The pads used were supplied by MOSIS and designed by California Technological University personnel. The input pads are nonbuffered, while the output pads are inverting.

Each of the chips was also designed to take advantage of one standard DAS 9200 Device Socket Card. As such, signals

common to every tiny chip are routed to the same pads. Figure 4.1 shows the standard frame used with the common signal assignments.

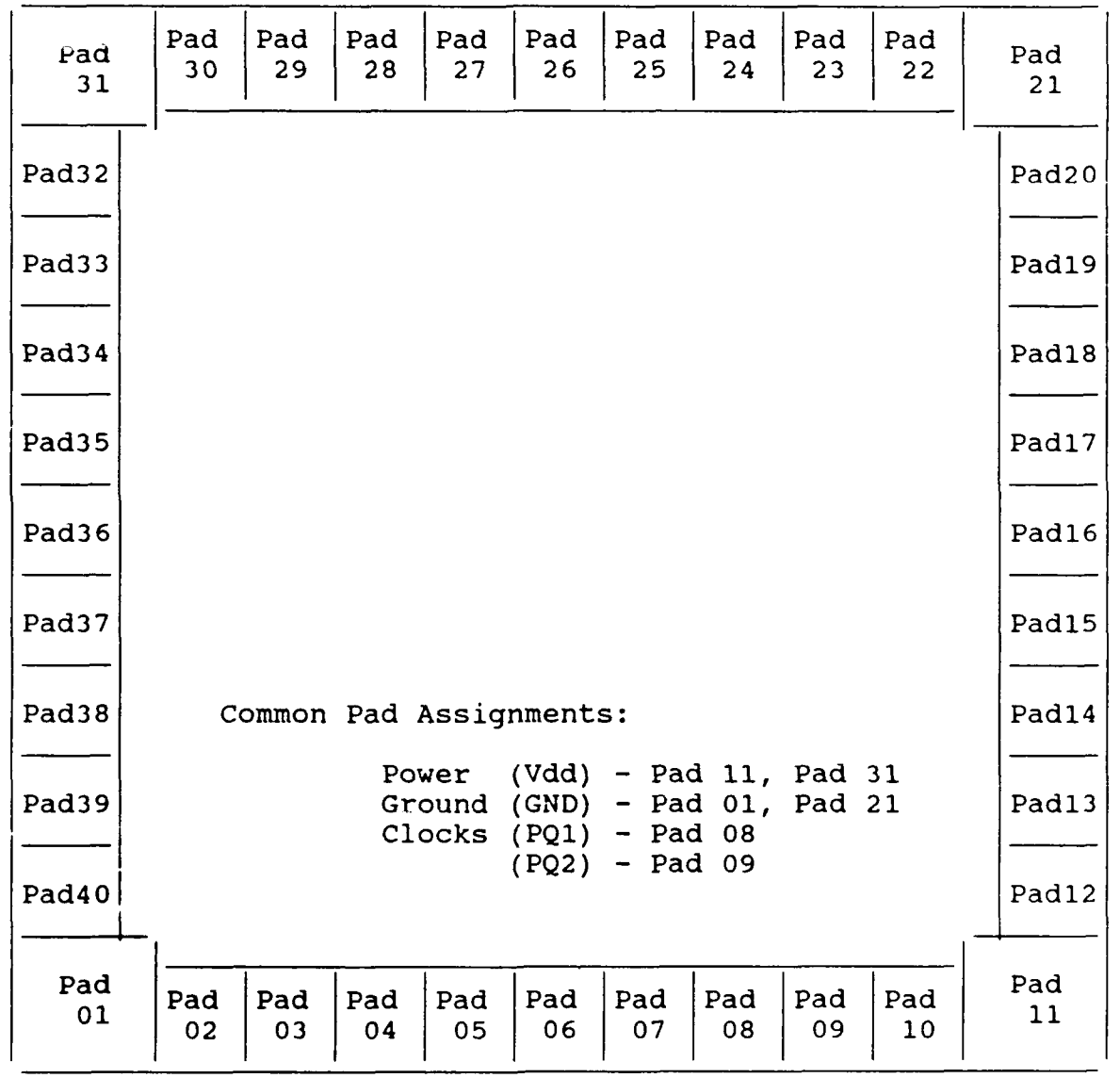


Figure 4.1: Standard Tiny Chip Pad Frame with Common Signal Assignments.

4.2.1 Register Tiny Chip. This tiny chip was designed to test a sample PISO register, a sample SIPO register, and each of the basic subcells associated with the two registers individually.

Each of the sample registers consist of a four by four register array surrounded by associated cells. The SIPO register receives its data inputs from parrnd cells and outputs its data to pads. As shown in table 4.1, all control

Table 4.1: Register tiny chip macrocell input/output pad assignment list.

Pad Name	Pad #	Data Signal Names SIPO Test	PISO Test
Inputs			
IZ00	2	sipo-0	piso-msb
IZ01	3	sipo-1	piso-2
IZ02	4	sipo-2	piso-1
IZ03	5	sipo-3	piso-lsb
IZ08	10	SDsipo'	SDpiso
IZ09	17		Lpiso
IZ10	18		SRpiso
IZ11	19	Lsipo	
IZ12	20	rcalc	
IZ13	22	pcalc'	
IZ14	23	par-append	
IZ15	24		parchk
IZ16	25		zerofill
IZ17	26		par-latch
IZ18	27		OPBAR
Outputs			
OZ00	12		data-out-a
OZ01	13		data-out-b
OZ02	14		data-out-c
OZ03	15		data-out-d
OZ11	37	data-out-a	
OZ12	38	data-out-b	
OZ13	39	data-out-c	
OZ14	40	data-out-d	

and input data signals are input to chip pads. The PISO register receives the same data as the SIPO as input to its four by four register. The data is then shifted to the parzer cells and output to pads. Again, all control and input data signals are input from chip pads.

Each of the basic subcells were placed such that no two cells shared common wells, though common signals, as shown in table 4.2, were shared to minimize routing problems and

Table 4.2: Register tiny chip individual cell test signal assignment list.

Pad Name	Pad #	Test Signal Names for Cells Associated with parrnd	sipo	piso	parzer
Inputs					
IZ00	2		par-data	ser-data	
IZ01	3	data-in	ser-data	par-data	data-in
IZ02	4	par-append'	Lsipo'	Lpiso'	zerofill'
IZ03	5	rcalc'	SDsipo	SDpiso'	parchk'
IZ04	6	phi1bar	phi1bar	phi1bar	phi1bar
IZ05	7	phi2bar	phi2bar	phi2bar	phi2bar
IZ08	10		SDsipo'	SDpiso	
IZ09	17			Lpiso	
IZ10	18			SRpiso	
IZ11	19		Lsipo	SRpiso'	
IZ12	20	rcalc			Vdd
IZ13	22	pcalc'			
IZ14	23	par-append			
IZ15	24				parchk
IZ16	25				zerofill
IZ17	26				par-latch
IZ18	27			Vdd	
IZ19	28		Vdd		
IZ20	29	Vdd			
Outputs					
OZ05	30				data-out
OZ06	32			serial-out	
OZ07	33			parallel-out	
OZ08	34		parallel-out		
OZ09	35		serial-out		
OZ10	36	data-out			

capacitances. In no case does one cell depend on another cell to function correctly as all required inputs to each cell are generated off chip and input as shown in table 4.2.

4.2.2 Preadd Tiny Chip. This tiny chip contains a complete WFTA16 preadd array, as well as a section containing individual adder/subtractor and associated cells for individual tests.

The preadd array accepts all primary inputs from off chip and sends all primary outputs to pads as shown in table 4.3.

Table 4.3: Preadd tiny chip input/output data signal assignment list.

Signal Name	Input Pad	Pad #	Signal Name	Output Pad	Pad #
reset-in	IZ00	2	reset-out	OZ05	20
h5 h14	IZ01	3	r210	OZ06	22
h13	IZ02	4	r211	OZ07	23
h4 h11	IZ03	5	r304	OZ08	24
h12 h15	IZ04	6	r305	OZ09	25
h3 h10	IZ05	7	r300	OZ10	26
h2 h9	IZ08	10	r301	OZ11	27
h1 h8	IZ09	11	r203	OZ12	28
h0 h7	IZ10	13	r212	OZ13	29
h6	IZ11	14	r213	OZ14	30
			r306	OZ15	32
			r209	OZ16	33
			r208	OZ17	34
			r307	OZ18	35
			r303	OZ19	36
			r302	OZ20	37
			r201	OZ21	38
			r109	OZ22	39
			r101	OZ23	40

The individual cell area contains one of each of the four cells required for a complete preadd array. Each of the cells are placed such that no wells are shared and such that, when testing individual cells, only one cell is functional at any time. No cell depends on another cell for any inputs as all cell inputs are generated off chip as shown in table 4.4. Also, all primary cell outputs are send to output pads.

Table 4.4: Preadd/Postadd tiny chip test cell input/output pad assignment list.

Pad Name	Pad #	Data Signal Names Test-A	Test-B	Test-C	Test-D
Inputs					
IZ00	2	reset			reset-in
IZ01	3	reset'			
IZ02	4	A		A	
IZ03	5	B			
IZ04	6	phi1bar		phi1bar	phi1bar
IZ05	7	phi2bar		phi2bar	phi2bar
IZ08	10	Vdd			
IZ09	12		Vdd		
IZ10	13			Vdd	
IZ11	14				Vdd
Outputs					
OZ00	15	diff-out	phi2bar		
OZ01	16	sum-out	phi1bar		
OZ02	17			data-out	reset'
OZ03	18				reset
OZ04	19				reset-out

Test-A: addsub-mine
Test-B: addsub-mine-inv
Test-C: addsub-mine-delay
Test-D: addsub-mine-end-cap

The individual cell area is also the same as on the preadd tiny chip.

4.2.3 Multiplier Test Cells Tiny Chip. This chip was designed to individually test each of the seven cells required for a complete multiplier array. An input/output pad test was also included as the pads used have not been tested before at AFIT and their operating parameters are not exactly known. Also, a sample controller PLA was added as space permitted.

Each multiplier cell is independently placed so no wells are shared with any other cell and separate power is supplied to each type of cell such that only one cell type operates at a time. Since space permitted, each cell has two separate occurrances. As shown in table 4.5, all cell inputs are generated off chip.

The associated multiplier cells are also independently placed and isolated from all other cells. Their inputs and outputs are as shown in table 4.6 as Test-J and Test-K.

The input/output pad test is merely an input pad attached directly to an output pad as specified in table 4.6, Test-M. A probe pad was placed along the metal line connecting the pads for parametric testing.

The sample controller PLA consists of an eight stage ringcounter, a PLA for control logic implemetation, and drivers. This controller implements the eight stage control function required for most WFTA operations. Though two

primary outputs are sent to pads as shown in table 4.7, Test-L, 16 probe pads were included for the testing of other signals.

Table 4.5: Multiplier Test Cells Tiny Chip Input/Output Data Signal Assignments - Multiplication Cells.

Pad Name	Pad #	Data Signal Names Test_E	Test-F	Test-G	Test-H	Test-I
Inputs						
IZ00	2	Vdd				
IZ01	3		Vdd			
IZ02	4			Vdd		
IZ03	5				Vdd	
IZ04	6	phi1bar	phi1bar	phi1bar	phi1bar	phi1bar
IZ05	7	phi2bar	phi2bar	phi2bar	phi2bar	phi2bar
IZ08	10					Vdd
IZ09	12	rstdc				rstdc
IZ10	13	SEc	SEc	SEc	SEc	SEc
IZ11	14	SE	SE	SE	SE	SE
IZ12	15	rstc	rstc			
IZ13	16				rst	rst
IZ14	17	data	data	data	data	data
IZ15	18	par-prod	par-prod	par-prod	par-prod	par-prod
Outputs						
OZ00	19	product				
OZ01	20		product			
OZ02	22			product		
OZ03	23				product	
OZ04	24					product

Test-E: mult-mine-2minus cell
Test-F: mult-mine-1minus cell
Test-G: mult-mine-0plus cell
Test-H: mult-mine-1plus cell
Test-I: mult-mine-2plus cell

Table 4.6: Multiplier Test Cells Tiny Chip Input/Output Data Signal Assignments - Auxiliary Multiplier Cells and PLA.

Pad Name	Pad #	Data Signal Names Test-J	Test-K	Test-L	Test-M
Inputs					
IZ04	6	phi1bar	phi1bar		
IZ05	7	phi2bar	phi2bar		
IZ13	16		control		
IZ16	28				pad-test-in
IZ17	29			OPR'	
IZ18	30		Vdd		
IZ19	39	Vdd			
Outputs					
OZ05	25			outcontrol	
OZ06	26			SDpiso	
OZ07	27				pad-test-out
OZ08	32	phi1bar			
OZ09	33	phi2bar			
OZ10	34		rstdc		
OZ11	35		SE		
OZ12	36		rstc		
OZ13	37		rst		
OZ14	38		control-out		
OZ15	39		SEc		

Test-J: mult-mine-inv cell
Test-K: mult-mine-end-cap cell
Test-L: 8stage controller
Test-M: Input/Output Pad Test

4.2.4 Multiplier Interface Tiny Chip. This tiny chip was designed to test the interfaces between all cells required for complete multiplier functioning. Every individual multiplier cell both accepts and transmits data to every other individual cell.

Only three chip specific inputs are required in addition to the inputs common to all chips as every multiplier set can

use the same two input data words and only one control bit is required as an input to the mult-mine-end-cap cell.

With five different multiplier cells, the number of possible chained combinations of cells is 25, so at least 25 primary outputs were required. The chip has 26 primary multiplier outputs as the multiply by one then minus two combination occurs twice. This extra set was added to allow the global routing lines within subcells to line up correctly. In a full multiplier array, which would be too large to place within a tiny chip, this condition would automatically be satified.

As well as the primary outputs, some secondary signals were routed to output pads as shown in table 4.7. These

Table 4.7: Multiplier Interface Tiny Chip Input/Output Data Signal Assignments.

Pad Name	Pad #	Signal Name	Pad Name	Pad #	Signal Name	Pad Name	Pad #	Signal Name
Inputs								
IZ02	10	multiplicand						
IZ03	12	partial-prod						
IZ04	13	control						
Outputs								
OZ00	2	(0+ 1+)	OZ10	18	phi1bar	OZ20	29	(2+ 2-)
OZ01	3	(0+ 2+)	OZ11	19	(0+ 0+)	OZ21	30	(1+ 2-)
OZ02	4	(1+ 2+)	OZ12	20	(1- 1-)	OZ22	32	(0+ 2-)
OZ03	5	(1+ 1+)	OZ13	22	(2- 2-)	OZ23	33	(1- 2-)
OZ04	6	(2+ 2+)	OZ14	23	(2+ 1+)	OZ24	34	(2- 1-)
OZ05	7	(1+ 2-)	OZ15	24	(2+ 0+)	OZ25	35	(2- 0+)
OZ06	14	phi1bar	OZ16	25	(1+ 0+)	OZ26	36	(2- 1+)
OZ07	15	phi2bar	OZ17	26	(2+ 1-)	OZ27	37	(2- 2+)
OZ08	16	signal	OZ18	27	(1+ 1-)	OZ28	38	(1- 0+)
OZ09	17	phi2bar	OZ19	28	(0+ 1-)	OZ29	39	(1- 1+)
						OZ30	40	(1- 2+)

secondary signals consist of inverted clock signals from the clock inverter (mult-mine-inv) cell and the internal data signal from a mult-mine-0plus cell.

4.2.5 Postadd Tiny Chip. Tnis tiny chip contains a complete WFTA16 postadd array, as well as a section containing individual adder/subtractor and associated cells for individual tests.

The postadd array accepts all primary inputs from off chip and sends all primary outputs to pads as shown in table 4.8.

Table 4.8: Postadd tiny chip input/output pad assignment list.

Signal Name	Input Pad	Pad #	Signal Name	Output Pad	Pad #
reset-in	IZ00	2	reset-out	OZ07	23
t3 t11	IZ01	3	h13	OZ08	24
t5	IZ02	4	h3	OZ09	25
t2 t15	IZ03	5	h5	OZ10	26
t6 t10	IZ04	6	h11	OZ11	27
t12 t16	IZ05	7	h9	OZ12	28
t17	IZ08	10	h7	OZ13	29
t8 t14	IZ09	11	h15	OZ14	30
t7	IZ10	12	h1	OZ15	32
t9	IZ11	13	h4	OZ16	33
t0 t4	IZ12	20	h12	OZ17	34
t1 t13	IZ13	21	h2	OZ18	35
			h14	OZ19	36
			h6	OZ20	37
			h10	OZ21	38
			h8	OZ22	39
			h0	OZ23	40

The individual cell area is identical to that found on

the preadd tiny chip as presented in section 4.4.2.

4.3 Tiny Chip Test Plan

The purpose of this section is to define the hardware and processes required to test each of the five tiny chips designed to characterize the performance of each of the arithmetic and register sections of a WFTA chip. The equipment that is common to each tiny chip test plan is discussed as well as the general test plan organization. Each of the test plans for the individual tiny chips are located in appendix C.

Three different types of tests were planned for each tiny chip. First, each tiny chip must under go a DC test to check for shorts between power and ground and to check for possible latch up problems. Second, each functional circuit must be functionally tested to determine the circuit's function as fabricated. And thirdly, functional circuits can be internally probed to help isolate errors discovered during earlier tests. This last test will not be discussed in detail as its requirements and procedures are based on the results of the previous tests.

4.3.1 Equipment. The three different sets of equipment listed in table 4.9 are required to test the tiny chips. One set of equipment is required to perform a DC power up test. The second set is required to perform functional and operational analysis. And the third set is required only if a

circuit fails the earlier tests and is used to probe individual circuits in an effort to find why it failed.

Table 4.9: Tiny Chip Test Equipment List.

DC Power up Test Equipment		
	Power Supply (0 to 5V, 5A)	1
	Digital Multimeter	2
	Integrated Circuit Protoboard	1
	Assorted Resistors and Wires	As needed
Functional and Operational Test Equipment		
	Power Supply (0 to 5V, 5A)	4
	DAS 9200, Digital Analysis System	1
	DAS 9201T, Color Monitor	1
	TF 100, Probe Station	1
	PHT-52, Device Socket Card	1
Circuit Probe Test Equipment		
	Power Supply (0 to 5V, 5A)	1
	Micromanipulator Work Station	1
	Micromanipulator Probes	4 or more
	Digital Pattern Generator	1
	Integrated Circuit Protoboard	1
	Various wires	As needed

4.3.2 DC Power up Test. This test is designed to find short circuits between power and ground and to find possible latch up problems within the tiny chip. Each tiny chip consists of multiple test circuits, each of which can be independently tested.

The basic procedure of this test is to ground each of the circuit's data, control, and clock input lines to ground through individual resistors. The tiny chip GND pads are then directly connected to ground. The Vdd pads are initially

connected to the power supply through a common, low ohmage resistor and an ammeter.

The power supply is then slowly run up from zero to five volts while the voltage drop across the input power resistor is monitored. If there is a significant voltage drop across the resistor, then a short exists between the Vdd and GND pads. Since the resistance between Vdd and GND in a CMOS circuit should be in the neighborhood of 10 Mohms, the voltage drop across the input resistor should be negligable.

If no shorts exist, the input resistor is removed and the power supply is connected directly to the Vdd pads through the ammeter. The power supply is then slowly run up from zero to five volts while the ammeter is observed for current spikes or cutoffs. If current spikes or cutoffs exist latch up may occur and care should be taken not to operate the circuit at the voltages where the problems occur.

Once the power supply is run all the way up to five volts, it should be turned off and the ammeter observed. If the ammeter shows a significant time is required for the current to drop off, latch-up is probably occuring.

4.3.3 Functional and Operational Tests. This test relies heavily on the DAS 9200 and associated equipment. Only one PHT-52, Device Socket Card, is required to test each tiny chip as the power, ground, and clock signals are input to each chip through the same pads and the Device Socket Card is wired

such that any of the remaining 34 pads can be used for input or output. The Device Socket Card tiny chip pad to probe wiring assignment is given in table 4.10 and is based on the same probe assignments as were used to test the WFTA16 chip.

Table 4.10: Generalized tiny chip pin to TF 100 probe position wiring assignments and reference clock wiring.

Pin	Acq Probe	Force Probe	Clk	Pin	Acq Probe	Force Probe	Pin	Acq Probe	Force Probe
1	GND			15	17-2	13-2	29	27-7	0-7
2	19-0	11-0		16	17-3	13-3	30	25-0	31-0
3	19-1	11-1		17	17-4	13-4	31	Vdd	
4	19-2	11-2		18	17-5	13-5	32	25-1	31-1
5	19-3	11-3	15-8	19	3-1	2-1	33	25-2	31-2
6	19-4	11-4	13-8	20	3-2	2-1	34	25-3	31-3
7			5-8	21	GND		35	25-4	31-4
8			3-8	22	27-0	0-0	36	25-5	31-5
9	19-5	11-5		23	27-1	0-1	37	25-6	31-6
10	19-6	11-6		24	27-2	0-2	38	25-7	31-7
11	Vdd			25	27-3	0-3	39	19-5	18-5
12	19-7	11-7		26	27-4	0-4	40	19-6	18-6
13	17-0	13-0		27	27-5	0-5			
14	17-1	13-1		28	27-6	0-6			

Reference Clock Connections

Reference Forcing Clock:	13-CLK
50% Duty Cycle Acquisition Clock:	19-CLK
Return to Zero Acquisition Clock:	17-8

Whether an individual pad is used for input or output is determined through the DAS 9200 Device Verification software in the Channel Allocation Menu. In all cases, device pads 8 and 9 are the primary return to zero clock, PHI1 and PHI2, inputs. Device pads 5 and 6 are the secondary return to one clock, phi1bar and phi2bar, inputs when individual cells are

being tested, but are used as normal level inputs when testing macrocells.

The functional test is initially run to determine if the cell being tested functions as anticipated. This test should be run at 1 Mhz. The operational test attempts to find the fastest speed at which the circuit will operate. For both tests, the clock period, pulse width, and delay times for both phases of the two phased clock are critical. The DAS 9200 is limited to a maximum operating frequency of 50 MHz. Also any clock signal must return to its base value, one or zero, at least 3 nsec prior to the end of a clock period. Table 4.11

Table 4.11: Operating period and clock pulse settings for DAS 9200 preprogrammed operating frequencies.

Operating Frequency	Period	Pulse Width	PHI2 Delay	PHI1 Delay
1 kHz	1 msec	80 nsec	5 nsec	99 nsec
2 kHz	500 usec	80 nsec	5 nsec	99 nsec
5 kHz	200 usec	80 nsec	5 nsec	99 nsec
10 kHz	100 usec	80 nsec	5 nsec	99 nsec
20 kHz	50 usec	80 nsec	5 nsec	99 nsec
50 kHz	20 usec	80 nsec	5 nsec	99 nsec
100 kHz	10 usec	80 nsec	5 nsec	99 nsec
200 kHz	5 usec	80 nsec	5 nsec	99 nsec
500 kHz	2 usec	80 nsec	5 nsec	99 nsec
1 MHz	1 usec	80 nsec	5 nsec	99 nsec
2 MHz	500 nsec	80 nsec	5 nsec	99 nsec
5 MHz	200 nsec	50 nsec	5 nsec	99 nsec
10 MHz	100 nsec	25 nsec	5 nsec	55 nsec
20 MHz	50 nsec	12 nsec	5 nsec	30 nsec
25 MHz	40 nsec	10 nsec	5 nsec	25 nsec
50 MHz	20 nsec	5 nsec	5 nsec	12 nsec

When required, the phi1bar pulse width and delay is the same as PHI1's and the phi2bar pulse width and delay is the same as PHI2's.

shows each of the DAS 9200 programmed operating frequencies, chip clock pulse widths and delays required for operations at those frequencies. As indicated in table 4.11, the minimum allowable pulse width is 5 nsec, the maximum pulse width is 80 nsec, and the maximum pulse delay is 99 nsec.

The operating frequencies are controlled through the period parameter included in the Run Contrcl Menu, while the pulse width, delay time, and whether the clock returns to zero (PHI1 and PHI2) or returns to one (phi1bar and phi2bar) are set within the Channel Allocation Menu.

To get a longer time spacing between PHI2 and PHI1, it would be necessary to operate the clocks separately in two different test vectors. This would double the size of any test pattern, but would increase the test's correspondence to the actual planned clocking scheme.

Initial testing should be done at a frequency of 1 MHz then adjusted up or down to determine maximum operating speed.

Since each tiny chip was designed such that as many cell primary outputs were wired to output pads as possible, the first test must be the input/output pad test on the multiplier test cells tiny chip. This is required to check the maximum performance levels of the pads as the potential limiting factor of test frequency measurements.

Test vectors and patterns should be generated using an event simulator such as the esim design tool.

4.3.4 Circuit Probe Test. This test is done only if a circuit failed its functional and operational test or if detailed timing parameters are required to be determined.

If a circuit fails its functional and operational test, it may be possible to probe intermediate data points using the micromanipulator. Not all cells can be probed. The magic files for each tiny chip must be consulted to determine what signals can be probed.

Since the probing looks for errors, error isolation techniques, such as those taught in the AFIT EENG 795 course, should be applied.

5. Conclusions and Recommendations

5.1 Testing and Test Environment

5.1.1 Overall Test Results. Using the Tektronix, DAS 9200, parts of the WFT16 chip were shown to be functioning correctly. The XROM and associated address generation and control circuitry were functioning correctly, as well as thc arithmetic and register control section. Also, the one-shot circuit used to initialize the WFT16 control section had to have worked as the chips showed the expected six clock cycle delay from the operate command to the first valid address being generated. In addition to the above, the parity calculate and append function done on output data was shown to be functioning correctly during both trivial and nontrivial transformation attempts.

The PISO register was shown to be performing consistantly even though the data MSBs were not being sign extended. Also, the control signal generation circuit operated as if it were independent of the scale factor inputs.

Overall, only the control section, less the scale factor dependency, was shown to be working as intended, while the PISO and SIPO registers have shown near expected operations. The other major sections, the preadder, multiplier, and postadder, were not tested enough to make any determinations as to how well they function.

The problems with the lack of scale factor dependency and

the lack of PISO sign extensions could be related to voltage biasing problems where n-transistors are not being turned off, thus allowing ground to be shorted to internal nodes.

5.1.2 Test Environment Improvements. Some testing was limited by the number of probes available to supply and sense signals. The entire XROM output address bus was ignored due to the lack of sufficient signal acquisition probes.

Equipment limitations also affected testing. With the normal maximum voltage swing at the stimulus probes being from 0.7 to 4.5 volts, the entire system ground had to be offset by -0.7 volts while the test chips remained at the normal ground. This meant the chip and the test system had to operate independently, with differing voltage references. This difference in references may be able to explain the lack of control section scale factor dependence and the lack of sign extensions in the PISO register.

To adequately perform functional testing on the WFT16 and future chips would require the test environment be upgraded. A new piece of equipment to replace the DAS 9200 would be expensive, but should be considered. The current system has a very limited ability to change configuration and has no ability to selectively jump from one section of a test pattern to another. These limitations mean that, once a chip test fixture is wired, any modification is a major one and any test which depends on the results of a previous test requires a

separate test pattern. Any new equipment should allow for quick configuration changes and test pattern jumping and looping without requiring multiple test patterns.

Still, due to the cost of new equipment, the DAS 9200 may remain the primary piece of test equipment. If this were the case, the minimum set of new equipment required to upgrade the tester would be stable, programmable power supplies powerful enough to handle the current and voltage requirements of both the test probes and the test chip. This equipment would replace old and unstable power supplies which have been marked as expendable, nonrepairable, and not calibratable.

5.2 Cell Library

With the improvements made in the cell library to standardize microcells and to automatically incorporate global routing, some attention should be turned to creating macrocells which are common to each of the WFT16, WFT17, and WFT15 circuits.

5.2.1 Common WFT Processor Data Path. Every WFT processor has an imaginary and real data side. Each of the two sides contain 24 output pads, 24 input pads, two clock pads, two power pads, two ground pads, a PISO register, a SIPO register, power, ground and clock busses, and input, output, test, and control data busses. These chip areas need not change from chip to chip.

The pad arrangement is already set. Any changes to the

existing arrangement would serve no functional purpose.

Each of the registers is already set to accomodate 24-bit words with the number of words dependent on the transform size, 15, 16, or 17 words. In any of the required processors, the 17 word registers could be used by simply ignoring or not using the unwanted outputs. The unwanted outputs could still be output to the test bus, but not used during normal operations.

The power, ground, and clock busses need not change from processor to processor. These busses should be laid out such that the arithmetic components of each processor have sufficient room to be placed between them. The WFT15 arithmetic section with five preadd stages, five postadd stages, and 13 multiplier stages would set the minimum separation distance between the busses.

The input, output, and test data busses can all be combined into one bus. By placing t-gates on the outputs of all functional areas and by placing buffers and t-gates along the bus itself, total functional isolation is possible. Through proper controlling of the t-gates and buffers, it would also be possible to connect any functional area to any other functional area as long as the data continued to flow through the circuit in a normal progression. The test function of this bus need not be limited to the input and output of data, but can include the input and output of

control signals. Only six of the 24 bus lines are required for PISO control, five are required for SIPO control, and only one is required for adder and multiplier control. The placement of this bus should circle the SIPO and PISO registers from the input pads to the output pads. The bus should run directly above the top of the registers leaving enough room between itself and the centerline of the processor to accomodate the 35 multipliers required for the WFT17.

The control data bus should be run along side one of the power busses in such a way that it can intersect with the test bus while it runs to the arithmetic and register sections. This bus should also contain the control signals for the functional area t-gates and the bus buffers and t-gates. Since the information this bus carries is identical on both the real and imaginary sides of the processor, the bus should interface with the control section right on the centerline of the processor. A separate centerline cell should be made to do this. This centerline cell would also accomodate the cross product terms required for the postadders.

5.2.2 Common WFT Processor Control. With each of the three planned processors, there are many control signals that change at the same times relative to either the beginning of a data cycle or the end of a data cycle. For instance, the latch PISO command always occurs during clock cycle zero of each data cycle, the shift down PISO commands occurs every odd

clock cycle, and the shift right PISO command always goes low during the last clock cycle of a data cycle. Also, the control signals required for XROM operations are exactly the same for all processor and cycles through its sequence every eight clock cycles.

In all three processors, no arithmetic or register signals are changing state, except the shift down PISO signal, during the middle six clock cycles of a data cycle. Since the shift down PISO signal switches state every clock cycle and no other signals change during the middle six clock cycles, a single 34 stage ring counter could be designed such that the two middle stages can be unused for a WFT16 controller and the four middle stages can be unused for a WFT15. Individualized PLAs would still have to be designed to take care of the scale factor dependent time lags in some signals.

This common section should also contain all the required input and output pads for the control section clocking and state variables, as well as the XROM address pads.

5.3 Design Verification

Custom VLSI efforts like the WFT16 involve placing 100,000 or more transistors and their associated metal lines, diffusion areas, and diffusion wells. The probability of total success on the first attempt is small. Also the cost of of fabricating a full scale custom VLSI circuit is very high.

An intermediate step, between a circuit's functional

design and its full scale fabrication, should be to break the circuit up into smaller components suitable for fabrication as tiny test chips which cost in the hundreds of dollars instead of the tens of thousands. To impliment and test a full scale WFT16 processor would require 40-pin tiny chips using 2 micron features as follows:

PISO Register	3 tiny chips
preadder	1 tiny chip
multiplier	6 tiny chips
postadder	1 tiny chip
SIPO Register	3 tiny chips
Control	1 tiny chip.

A full scale XROM would be too large to fabricate on a tiny chip and the use of multiple tiny chips may not be practical.

A divide and conquer approach as above would allow for a relatively inexpensive charactorization of a full processor while validating microcells, functional subsections, and timing.

5.4 VLSI Program Management

In the five years of the AFIT WFTA project, all project work can be fit into the seven general catagories of theory validation, system architecture specification, component design, circuit integration, circuit simulation, prototype fabrication, and prototype testing.

Theory validation in 1985 showed the project was feasible using the Winograd small and large Fourier transform algorithms. The system architecture specification and

component designs done in 1985 and 1986 showed it was possible to integrate 15-, 16-, and 17-point processors onto single chips and to interface them with separate memories, a master controller, and a host computer. Work then progressed to fabricate a prototype 16-point processor for testing.

Through its five year life, only component verification has been missing as a catagory of work progress. The five tiny test chips designed as part of this thesis will fill in that gap. But something else has been missing, something that affects all stages and areas of project work. That missing ingrediant is a clear, focused, and realistic goal. Up to now, the project goal has been to make a 4080-point Winograd Fourier transform processor as small and fast as possible, then worry about how to used it later. Though this goal has been shown to be attainable, it is not realistic. It is incumbent upon interested faculty members and students to determine the actual uses of such a processor and to carry on project work toward those uses. As it is, the project can be carried out to its current goal, then be found incompatable or over qualified for possible uses.

Appendix A

Control Signal Definitions

A1 PISO Register Control Signals

a. SDpiso (Shift Down PISO) - When this signal is high, the input parallel data is shifted away from the initial row of PISO cells. The signal goes high every other clock cycle and corresponds with the second clock cycle in which the input data bus is stable. The input data can change with the beginning of the next clock cycle. This is the same signal as SDsipo'.

b. Lpiso (Latch PISO) - When this signal is high, the 24-bit parallel input data words are latched into the serial output paths of the PISO. This signal must occur for only one clock cycle immediately after the parallel side of the register is full of valid data. This signal cannot be set high at any time when SDpiso or SRpiso are high.

c. SRpiso (Shift Right PISO) - When this signal is high, the data stored in the serial path of the register is shifted away from the register's MSB end and toward the parity check/zerofill (parzer) cell end of the register. This signal must go high during the last clock cycle during which a zero is appended as an LSB of the data word. This overlap causes the input data parity bit to be stripped from the data before it goes to the preadder. The signal then stays high, going low on the same clock cycle as when Lpiso goes high

d. parchk (Parity Check) - When this signal is high, the parity of each of the input data words is checked for odd parity. This signal goes high at the same time as SRpiso and goes low after 24 complete clock cycles.

e. par-latch (Parity Latch) - This signal goes high for one clock cycle corresponding with the last clock cycle the parchk signal is high. This signal causes the calculated parity of each of the input data words to be sensed through a pulldown network. If any of the data words were of even parity, the network would be pulled down and the Parity Error flag bit would be switched on.

f. zerofill (Zerofill) - This signal goes high the clock cycle after the Lpiso signal and stays high depending on the scale factor input to the WFTA circuit before operations began. In no case will this signal last less than one clock cycle as a one clock cycle overlap with SRpiso is required to strip the parity bit off the input data words.

g. OPBAR (Operate complement) - This signal goes low whenever the Operate command sent to the WFTA circuit is high. This allows the parity information sensed while the par-latch signal is high to be passed to the Parity Error flag bit. When this signal is high, the circuit is not in operating mode and the Parity Error flag bit is then set low regardless of any other operations.

A2 Arithmetic Section Control Signals

a. reset (Reset Adders/Reset Multipliers) - When this signal goes low, the carry bit of each adder is reset to zero and the carry bit of each subtractor is reset to one. This one clock cycle long low signal propagates through the bit serial adder section at the same time as the data MSB. This signal enters the arithmetic section at the preadder stage with the data MSB comming from the parzer bank. It is then propagated, with the data MSBs, to the multiplier array and then to the postadder stage.

b. mround (Multiply Round) - This signal controls the rounding circuit used after the multipliers and before the postadders. The intermediate results are rounded to 30 bits. This signal goes high for the two clock cycles in which the two LSBs of each data word leave the multiplier array. This signal is used in the fabricated WFTA16 only.

A3 SIPO Register Control Signals

a. rcalc (Calculate Rounded Data) - While this signal is low, the carry bit within the parrnd cell adder is set to the incomming bit from the arithmetic section. This sets up the rounding of the data word's 23 MSBs by adding the 23rd and 24th MSBs together then adding the resulting carry to the next bit while generating a new carry and so on. The signal stays high for 23 clock cycles.

b. pcalc' (Parity Calculate complement) - While this signal is low the parrnd cell parity checking circuit is non-operational. When this signal goes high the parrnd cell calculates the parity of each of the 23-bit rounded data words comming from the parrnd adder circuit. This signal goes high one clock cycle after rcalc, then goes low again one clock cycle after rcalc.

c. par-append (Parity Append) - This signal goes high for only the one clock cycle after the pcalc' signal goes transistions low. When this signal is high, the calculated parity of the data word is sensed and the proper valued bit is added to the data as its MSB to ensure odd parity.

d. Lsipo (Latch SIPO) - This signal goes high for the one clock cycle after the par-append signal. When the signal is high, the data in the SIPO register is transfered from the serial path to the parallel path of the register. This signal cannot be high at the same time as the SDsipo' signal is low.

e. SDsipo' (Shift Down SIPO complement) - When this signal is low, the parallel data in the register is shifted toward the output cells of the register. This is the same signal as SDpiso.

Appendix B

Basic WFTA Cell Descriptions

B1. Parallel-in Serial-out Register Cells

B1.1 Introduction

The PISO register is designed to accept one 24-bit long data word every second clock cycle for 32 clock cycles, then translate the data into 16 32-bit serial data words by shifting the data out through the parity error checking and zerofill cell by adding zeros as the data word's LSBs and extending the data word's sign as required by the scale factor bits input to the circuit prior to operations beginning.

B1.2 Individual PISO Cells

B1.2.1 piso-mine

1. Dimensions: Height - 72 lambda
   Width - 104 lambda
2. Input Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      SDpiso SDpiso'
      SRpiso SRpiso'
      Lpiso Lpiso'
   c. Data
      piso-par-in
      piso-ser-in
3. Output Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      SDpiso SDpiso'
      SRpiso SRpiso'
      Lpiso Lpiso'
   c. Data
      piso-ser-out
      piso-par-out
4. Operation

   Parallel Data - With every second clock cycle, the parallel data is accepted from the previous piso-mine cell then placed in a master slave flip-flop and readied for output. The output remains valid for two clock cycles, but the

next piso-mine cell will only accept data every second clock cycle based on the SDpiso signal going high.

Latching Data - Once a piso register is completely loaded with valid parallel data, the Lpiso control signal goes high and the parallel data stored in a cell is transfered, within the cell, to serial data. The Lpiso and the SDpiso signals cannot be high at the same time.

Serial Data - With every clock cycle, when the SRpiso control signal is high, the serial data is accepted from the previous piso-mine cell then placed in a master slave flip-flop and readied for output to the next piso-mine cell at the beginning of the next clock cycle.

B1.2.2 piso-mine-msb

1. Dimensions: Height - 72 lambda
   Width - 104 lambda

2. Input Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      SDpiso SDpiso'
      SRpiso SRpiso'
      Lpiso Lpiso'
   c. Data
      piso-par-in

3. Output Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      SDpiso SDpiso'
      SRpiso SRpiso'
      Lpiso Lpiso'

4. Operation

Parallel Data - This cell treats parallel data exactly the same as the piso-mine cell.

Latching Data - This cell treats the latching of parallel to serial data the same as the piso-

mine cell.

Serial Data - This cell treats serial data the same as the piso-mine cell except for the serial input. This cell has its serial input wired to its serial output, through a t-gate on SRpiso, to automatically generate data word sign extensions.

Sign Extentions - Since only 24 bit long data words are input to a WFTA chip but the data words being processed are longer than 24 bits, the input data word's most significant or sign bit must be extended to fill the full word length. This is automatically accomplished when the SRpiso signal goes low and opens a feedback t-gate to the serial input to the cell.

5. Notes - This cell is designed such that its left edge can butt up against the right edge of both the sipo-mine and sipo-mine-out cells. This allows the SIPO and PISO registers to be placed directly adjacent without any additional layout having to be done.

B1.2.3 piso-mine-inv

1. Dimensions: Height - 116 lambda
   Width - 208 lambda

2. Input Signals
   a. Clocks
      PQ1
      PQ2
   b. Control - none
   c. Data
      piso-data-A (from input pad)
      piso-data-B (from input pad)

3. Output Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control - none
   c. Data
      piso-data-A (to piso cell)
      piso-data-B (to piso cell)

4. Operation - This cell is used to generate the phi1bar and phi2bar clock signals required for the

piso-mine and piso-mine-msb cell clocking. The cell also serves to automatically route power and ground to the piso-mine and piso-mine-msb cells as well as global power, ground, and clocks. The cell interfaces with the sipo-mine-inv and parzer-mine-inv cell power, ground, and clock lines.

B1.2.4 piso-mine-end-cap

1. Dimensions: Height - 166 lambda
   Width - 104 lambda

2. Input Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      SDpiso
      SRpiso
      Lpiso
   c. Data - none

3. Output Signals
   a. Clocks - none
   b. Control
      SDpiso SDpiso'
      SRpiso SRpiso'
      Lpiso Lpiso'
   c. Data - none

4. Operation - This cell is used to generate the SDpiso complement and Lpiso complement control signals. It also routs the required control signals, as well as power and ground, to the piso-mine and piso-mine-msb cells. Global routing of power; ground; and parrnd-mine, sipo-mine(-out), and piso-mine(-msb) control signals is also accomplished through the interfacing with the sipo-mine-end-cap and parzer-mine-end-cap cells.

B1.2.5 parzer-mine

1. Dimensions: Height - 72 lambda
   Width - 205 lambda

2. Input Signals
   a. Clock
      PQ1 phi1bar
      PQ2 phi2bar

b. Control
   parchk parchk'
   zerofill zerofill'
   par-latch
c. Data
   piso-ser-out

3. Output Signals
   a. Clock
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      parchk parchk'
      zerofill zerofill'
      par-latch
   c. Data
      parzer-data-out (to pre-adders)
      parerrbar (pulldown only to parzer-mine-end-cap cell)

4. Operation

Zerofilling - When the zerofill control signal is high, the parzer-data-out signal is tied to ground to output logical zeros. This extension of a data word by adding zeros as the least significant bits is required if too many sign extensions would be required to do the same function. The zerofill control signal can stay high for multiple clock cycles and must be high for at least one clock cycle. Overlapping the zerofill control signal during its last clock cycle high are the parchk and SRpiso control signals. When the zerofill signal goes low, the data input from the piso-mine cell is passed through to the pre-adders.

Parity Checking - The parchk signal remains high for 24 clock cycles. During this time, the serial data from the piso-mine cell is checked for parity. Also since this signal and zerofill over lap by one clock cycle, the data word's least significant or parity bit is truncated and not used in further data processing.

Flagging Parity Errors - Once the data word's parity has been determined, the par-latch control signal goes high for one clock cycle. If the word's parity was even, then the parerrbar output signal is pulled down. This is the result of a input parity error.

B1.2.6 parzer-mine-inv

1. Dimensions: Height - 116 lambda
   Width - 205 lambda

2. Input Signals
   a. Clocks
      PQ1
      PQ2
   b. Control - none
   c. Data - none

3. Output Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control - none
   c. Data - none

4. Operation - This cell is used to generate the phi1bar and phi2bar clock signals required for the parzer-mine cell clocking. The cell also serves to automatically route power and ground to the parzer-mine cells as well as global power, ground, and clocks. The cell interfaces with the piso-mine-inv cell power, ground, and clock lines.

B1.2.7 parzer-mine-end-cap

1. Dimensions: Height - 216 lambda
   Width - 250 lambda

2. Input Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      parchk
      zerofill
      par-latch
      OPBAR
   c. Data - none

3. Output Signals
   a. Clocks - none
   b. Control
      parchk parchk'
      zerofill zerofill'
      par-latch
      OPBAR

c. Data - none

4. Operation - This cell generates the parchk complement and zerofill complement control signals used in the parzer-mine cells. The cell also provides the parzer-mine cells with all the required control signals. Contained within the cell is the parerr-mine cell used to output a flag if any of the data words input to the system are of even parity. Global routing of power; ground; and parrnd-mine, sipo-mine(-out), piso-mine(-msb), and parzer-mine control signals is also accomplished through the interfacing with the piso-mine-end-cap cell.

B1.2.8 parerr-mine

1. Dimensions: Height - 39 lambda
   Width - 81 lambda

2. Input Signals
   a. Clocks - none
   b. Control
      par-latch
      OPBAR
   c. Data
      parerrbar

3. Output Signals
   a. Clocks - none
   b. Control
      par-latch
   c. Data
      parerr-bit (to output pads)

4. Operation - This cell only functions when the chip is the chip is in operating mode as opposed to watchdog mode. The output is a continuous zero except when par-latch goes high and one of the parzer-mine cells draws the parerrbar input line low. If no parity errors are found on the input data, the parerr-bit will remain zero.

5. Comment - This cell is wholly contained within the parzer-mine-end-cap cell.

B1.3 PISO Register Construction.

To construct an n-word by m-bit PISO register, where m is even, the following steps should be followed:

1. Array the piso-mine-inv cells 1 high by m/2 long.

2. Place a piso-mine-msb cell flush with the top left edge of the piso-mine-inv array. Array the piso-mine-msb cell n high by 1 long.

3. Place a piso-mine cell flush with the top of the left most piso-mine-inv cell and the right edge of the piso-mine-msb cell. Array the piso-mine cell n high by m-1 long.

4. Place a piso-mine-end-cap cell flush with the top left edge of the top most piso-mine-msb cell. Array the piso-mine-end-cap cell 1 high by m long.

5. Place a parzer-mine-inv cell flush with the bottom right side of the right most piso-mine-inv cell.

6. Place a parzer-mine cell directly on top of the parzer-mine-inv cell, flush with the piso-mine array. Array the parzer-mine cell n high by 1 long.

7. Place a parzer-mine-end-cap cell flush with the top of the top most parzer-mine cell and the right right edge of the right most piso-mine-end-cap cell.

B2. Adder/subtractor Cells

B2.1 Introduction

The adder/subtractors are designed to serially add and subtract data words. This addition is done at the rate of one bit per clock cycle per cell.

B2.2 Individual Adder/subtractor Cells

B2.2.1 addsub-mine

1. Dimensions: Height - 132 lambda
   Width - 219 lambda

2. Input Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      reset
   c. Data
      A
      B

3. Output Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      reset
   c. Data
      sum (A + B)
      diff (A - B)

4. Operation - This cell takes two bits of data each clock cycle. It adds and subtracts the bits from each other with the previous carry or borrow bits. The next carry and borrow bits are generated at the same time as the sum and difference. The four generated bits are then fed through master slave flip-flops with the sum and difference bits moving on to the next cell, while the carry and borrow bits are fed back for the next cycle. When the reset signal goes high, the carry bit is reset to zero while the borrow bit is reset to one.

B2.2.2 addsub-mine-delay

1. Dimensions: Height - 44 lambda
   Width - 219 lambda

2. Input Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      reset
   c. Data
      data-in

3. Output Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      reset
   c. Data
      data-out

4. Operation - This cell takes one bit of data each clock cycle, holds it in a master slave flip-flop, outputs it with the rise of PQ1 to the next cell.

B2.2.3 addsub-mine-delay-null

1. Dimensions: Height - 44 lambda
   Width - 219 lambda

2. Input Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      reset
   c. Data - none

3. Output Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      reset
   c. Data - none

4. Operation - This cell serves as a filler cell dto carry power, ground, clock, and reset signals

down an addsub column. By placing this cell within a column, the top most and bottom most cells of each required column can be made to line up, thus making global routing of power, ground, and clock trivial.

B2.2.4 addsub-mine-inv

1. Dimensions: Height - 126 lambda
   Width - 219 lambda

2. Input Signals
   a. Clocks
      PQ1
      PQ2
   b. Control - none
   c. Data - none

3. Output Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control - none
   c. Data - none

4. Operation - This cell is used to generate the phi1bar and phi2bar clock signals required for the addsub-mine and addsub-mine-delay cell clocking. The cell also serves to automatically route power and ground to those cells as well as global power, ground, and clocks.

B2.2.5 addsub-mine-end-cap

1. Dimensions: Height - 93 lambda
   Width - 219 lambda

2. Input Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      reset-adders
   c. Data - none

3. Output Signals
   a. Clocks - none

b. Control
reset-adders (delayed one clock cycle)
reset
c. Data - none

4. Operation - This cell generates the reset control signal to reset the addsub-mine cell carry and borrow bits. The cell also contains the global routing of power and ground.

B2.3 Adder/subtractor Column Construction

To build a column of bit serial adders that are all reset at the same time, the following steps should be followed:

1. Place an addsub-mine-inv cell at a chosen point.

2. Place an addsub-mine or addsub-mine-delay cell directly on top of the addsub-mine-inv cell flush with both the left and right sides.

3. Place an addsub-mine or addsub-mine-delay cell directly on top of the previous cell and flush with the left and right sides.

4. Repeat step 3 until all required addsub-mine and addsub-mine-delay cells have been laid out.

5. Place an addsub-mine-end-cap directly on top of the previous cell and flush with the left and right sides.

If multiple adds are required, then multiple addsub columns will be required. To facilitate the routing of the global power, ground, and clocks, addsub-mine-delay-null cells can be inserted into columns to allow the addsub-mine-inv cells and addsub-mine-end-cap cells to line up so the power, ground, and clock signals can be simply brought straight across without corners.

B3. Multiplier Cells

B3.1 Introduction

The WFTA multiplier cells are designed to implement the Booth's Quatenary Algorithm on bit serial data as constant multiplier values. Each of the five multiplier cells has two data inputs and two data outputs. Each multiplier cell is basically the same as the other multiplier cells with just minor variations to implement the required data delays and whether the cell adds or subtracts.

B3.2 Individual Multiplier Cells

B3.2.1 mult-mine-0plus

1. Dimensions: Height - 87 lambda
   Width - 297 lambda
2. Input Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      rst rstc (reset carry bit)
      rstdc (force a zero into adder)
      SE SEc (sign extensions)
   c. Data
      multiplicand
      PPI (partial product)
3. Output Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      rst rstc
      rstdc
      SE SEc
   c. Data
      multiplicand (delayed 3 clock cycles)
      product (partial product)
4. Operation - This cell performs no function other than to delay the multiplicand data by three clock cycles and to delay the partial product by one clock cycle and add two sign extensions. These delays set the data up so the timing is correct for the next cell to properly process the data.

B3.2.2 mult-mine-2plus

Dimensions: Height - 87 lambda
Width - 297 lambda

2. Input Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      rst rstc (reset carry bit)
      rstdc (force a zero into adder)
      SE SEc (sign extensions)
   c. Data
      multiplicand
      PPI (partial product)

3. Output Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      rst rstc
      rstdc
      SE SEc
   c. Data
      multiplicand (delayed 3 clock cycles)
      product (partial product)

4. Operation - This cell adds the multiplicand data after two clock cycle delays to the partial product data. The multiplicand data is then delayed one more clock cycle before being output to the next cell. The new partial product bit is calculated and output one clock cycle later. Also, the partial product's sign bit is extended twice after the final addition. When the rst signal goes high, the carry bit in the adder is reset to zero.

B3.2.3 mult-mine-1plus

1. Dimensions: Height - 87 lambda
   Width - 297 lambda
2. Input Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar

b. Control

rst	rstc	(reset carry bit)
rstdc		(force a zero into adder)
SE	SEc	(sign extensions)

c. Data

multiplicand
PPI (partial product)

3. Output Signals
   a. Clocks

PQ1	phi1bar
PQ2	phi2bar

   b. Control

rst	rstc
rstdc	
SE	SEc

   c. Data

multiplicand (delayed 3 clock cycles)
product (partial product)

4. Operation - This cell adds the multiplicand data after one clock cycle delay to the partial product data. The multiplicand data is then delayed two more clock cycles before being output to the next cell. The new partial product bit is calculated and output one clock cycle later. Also, the partial product's sign bit is extended twice after the final addition. When the rst signal goes high, the carry bit in the adder is reset to zero.

B3.2.4 mult-mine-1minus

1. Dimensions: Height - 87 lambda
   Width - 297 lambda
2. Input Signals
   a. Clocks

PQ1	phi1bar
PQ2	phi2bar

   b. Control

rst	rstc	(reset carry bit)
rstdc		(force a zero into adder)
SE	SEc	(sign extensions)

   c. Data

multiplicand
PPI (partial product)

3. Output Signals
   a. Clocks

PQ1	phi1bar
PQ2	phi2bar

b. Control

rst	rstc
rstdc	
SE	SEc

c. Data

multiplicand (delayed 3 clock cycles)
product (partial product)

4. Operation - This cell adds the complemented multiplicand data after one clock cycle delay to the partial product data. The multiplicand data is then delayed two more clock cycles before being output to the next cell. The new partial product bit is calculated and output one clock cycle later. Also, the partial product's sign bit is extended twice after the final addition. When the rst signal goes high, the carry bit in the adder is reset to one to implement a two's complement of the delayed multiplicand.

B3.2.5 mult-mine-2minus

1. Dimensions: Height - 87 lambda
   Width - 297 lambda
2. Input Signals
   a. Clocks

PQ1	phi1bar
PQ2	phi2bar

   b. Control

rst	rstc	(reset carry bit)
rstdc		(force a zero into adder)
SE	SEc	(sign extensions)

   c. Data

multiplicand
PPI (partial product)

3. Output Signals
   a. Clocks

PQ1	phi1bar
PQ2	phi2bar

   b. Control

rst	rstc
rstdc	
SE	SEc

   c. Data

multiplicand (delayed 3 clock cycles)
product (partial product)

4. Operation - This cell adds the complemented multiplicand data after two clock cycle delays to

the partial product data. The multiplicand data is then delayed one more clock cycle before being output to the next cell. The new partial product bit is calculated and output one clock cycle later. Also, the partial product's sign bit is extended twice after the final addition. When the rst signal goes high, the carry bit in the adder is reset to one to implement a two's complement of the delayed multiplicand.

B3.2.6 mult-mine-inv

1. Dimensions: Height - 104 lambda
   Width - 297 lambda
2. Input Signals
   a. Clocks
      PQ1
      PQ2
   b. Control - none
   c. Data - none

3. Output Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control - none
   c. Data - none

4. Operation - This cell generates the phi1bar and phi2bar clock signals required for multiplier operations. The cell also automatically handles the routing of global power, ground, and clock signals.

B3.2.7 mult-mine-end-cap

1. Dimensions: Height - 87 lambda
   Width - 297 lambda
2. Input Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      reset-mult (same as reset-adders)
   c. Data - none

3. Output Signals
   a. Clocks - none

b. Control

reset-mult (delayed one clock cycle)
rst rstc
rstdc
SE SEc

c. Data - none

4. Operation - This cell generates all control signals being sent to the multiplier cells. When the reset-mult signal goes low, the carry bits are reset by the rst signal, a zero is sent into the adder by the rsdc signal, and two sign extensions are added to the the partial product by the SE signal.

B3.3 Multiplier Construction

To construct a multiplier array with n-words by m-stages based on Booth's Quatenary Algorithm, the following steps should be followed:

1. Place a mult-mine-inv cell within the layout and array it 1 high by m long.

2. Place the cell corresponding to the most significant multiplication directly on top of the left most mult-mine-inv cell flush with both left and right sides.

3. Place the next most significant cell directly to the right of the previous multiplier cell. Continue this until all m cell have been laid out.

4. Connect the right most partial product data input (PPI) to ground.

5. Repeat steps 2 through 4 by stacking cells directly on top of previous multiplication cells until all n-words have been implimented.

6. Place a mult-mine-end-cap cell directly on top of the top most significant cell and array it 1 high by m long.

B4. Serial-in Parrallel-out Register Cells

B4.1 Introduction

The SIPO register is designed to accept serial data of length m and round it down to data of length n, where m > n, while checking the parity on the rounded data. The rounded data is shifted into the sipo register cells. After all n bits are shifted in, a parity bit is shifted in as each data word's msb to make each outpout data word have odd parity. The data in then shifted out of the register one word at a time in parallel.

4.2 Individual SIPO Cells

4.2.1 parrnd-mine

1. Dimensions: Height - 72 lambda
   Width - 263 lambda

2. Input Signals:
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      rcalc rcalc'
      pcalc'
      par-append par-append'
   c. Data
      data-in

3. Output Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      rcalc rcalc'
      pcalc'
      par-append par-append'
   c. Data
      data-out

4. Operation - Serial data is accepted from the last stage of the post-adders. The data word is serially rounded to its 23 most significant bits by adding one to the data's 24th most significant bit then adding the resultant carry to the 23rd most significant bit. The resultant carry is then added to the 22nd most significant bit and so on. Overflow is not a problem as the only time a sign

could change is if the input data word has all ones in its 24 most significant bits and would then be rounded to a data value of zero. The rounded result is then checked for odd parity while also being input to the sipo register. Once the entire rounded 23 bit word is input to the sipo register a 24th bit is then input to the sipo register to make the entire 24 bit word odd in parity.

B4.2.2 parrnd-mine-inv

1. Dimensions: Height - 116 lambda
   Width - 263 lambda

2. Input Signals:
   a. Clocks
      PQ1
      PQ2
   b. Control - none
   c. Data - none

3. Output Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control - none
   c. Data - none

4. Operation - This cell generates the phi1bar and phi2bar clock signals required for theparrnd-mine cells to operate as well as supplying the global routing of the power, ground, and clock signals. The cell interfaces with the sipo-mine-inv cell power, ground, and clock lines.

4.2.3 parrnd-mine-end-cap

1. Dimensions: Height - 166 lambda
   Width - 263 lambda

2. Input Signals:
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      rcalc
      pcalc'
      par-append

c. Data - none

3. Output Signals
   a. Clocks - none
   b. Control

rcalc	rcalc'
pcalc'	
par-append	par-append'

   c. Data - none

4. Operation - This cell is used to generate the complements of the Round Calculate and Parity Append control signals. It also routs the required control signals, as well as power and ground, to the parrnd-mine cells. Global routing of power, ground, and parrnd-mine control signals is also accomplished. The cell interfaces with sipo-mine-end-cap.

4.2.4 sipo-mine

1. Dimensions: Height - 72 lambda
   Width - 104 lambda

2. Input Signals
   a. Clocks

PQ1	phi1bar
PQ2	phi2bar

   b. Control

SDsipo	SDsipo'
Lsipo	Lsipo'

   c. Data
      sipo-ser-in
      sipo-par-in

3. Output Signals
   a. Clocks

PQ1	phi1bar
PQ2	phi2bar

   b. Control

SDsipo	SDsipo'
Lsipo	Lsipo'

   c. Data
      sipo-ser-out
      sipo-par-out

4. Operation

Serial Data - With every clock cycle, the serial data is accepted from the previous sipo-

mine or parrnd-mine cell then placed in a master slave flip-flop and readied for output to the next sipo-mine cell at the beginning of the next cycle.

Parallel Data - With every second clock cycle, the parallel data is accepted from the previous sipo-mine cell then placed in a master slave flip-flop and readied for output. The output remains valid for two clock cycles, but the next sipo-mine or sipo-mine-out cell will only accept data every second clock cycle based on the Shift Down sipo signal going high.

Latching Data - Once a sipo register is completely loaded with valid serial data, the Latch sipo (Lsipo) control signal goes high and the serial data stored in a cell is transfered, within the cell, to parallel data. The Latch sipo and the Shift Down sipo signals cannot be high at the same time.

4.2.5 sipo-mine-out

1. Dimensions: Height - 72 lambda
   Width - 104 lambda

2. Input Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      SDsipo SDsipo'
      Lsipo Lsipo'
   c. Data
      sipo-ser-in
      sipo-par-in

3. Output Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      SDsipo SDsipo'
      Lsipo Lsipo'
   c. Data
      sipo-ser-out
      sipo-data-out

4. Operation

Serial Data - Serial data is treated the same as for the sipo-mine cell.

Parallel Data - Parallel data is treated the same as for the sipo-mine cell with the exception that the parallel data out is sent to the output pads and not another sipo cell.

Latching Data - Latching data is treated the same as for the sipo-mine cell.

5. Notes - The sipo-mine-out cell is the same as the sipo-mine cell with the exception of the parallel data output inverter being twice as wide and the parallel data output signal leaves the cell via a metal 2 line since it doesn't need to provide data to any other sipo register cell.

4.2.6 sipo-mine-inv

1. Dimensions: Height - 116 lambda
   Width - 208 lambda

2. Input Signals
   a. Clocks
      PQ1
      PQ2
   b. Control - none
   c. Data
      sipo-data-A (from sipo-mine-out cell)
      sipo-data-B (from sipo-mine-out cell)

3. Output Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control - none
   c. Data
      sipo-data-A (to output pads)
      sipo-data-B (to output pads)

4. Operation - This cell is used to generate the phi1bar and phi2bar clock signals required for the sipo-mine and sipo-mine-out cell clocking. The cell also serves to automatically route power and ground to the sipo-mine and sipo-mine-out cells as well as global power, ground, and clocks. The cell interfaces with the parrnd-mine-inv and piso-

mine-inv cell power, ground, and clock lines.

4.2.7 sipo-mine-end-cap

1. Dimensions: Height - 166 lambda
   Width - 104 lambda

2. Input Signals
   a. Clocks
      PQ1 phi1bar
      PQ2 phi2bar
   b. Control
      SDsipo'
      Lsipo
   c. Data - none

3. Output Signals
   a. Clocks - none
   b. Control
      SDsipo SDsipo'
      Lsipo Lsipo'
   c. Data - none

4. Operation - This cell is used to generate the Shift Down sipo and Latch sipo complement control signals. It also routs the required control signals, as well as power and ground, to the sipo-mine and sipo-mine-out cells. Global routing of power, ground, and parrnd-mine and sipo-mine(-out) control signals is also accomplished through the interfacing with the parrnd-mine-end-cap and piso-mine-end-cap cells.

4.3 SIPO Register Construction

To construct an n-word by m-bit (m is even) SIPO reigster, the following steps should be followed:

1. Place a parrnd-mine-inv cell in the layout.

2. Place a parrnd-mine cell directly on top the parrnd-mine-inv cell and array it n high by 1 long.

3. Place a parrnd-mine-end-cap cell directly on top of the top most parrnd cell.

4. Place a sipo-mine-inv cell flush with the right edge of the parrnd-mine-inv cell such that the upper right corner of the parrnd-mine-inv cell touches the upper left corner of the sipo-

mine-inv cell. Array the sipo-mine-inv cell 1 high by m/2 long.

5. Place a sipo-mine-out cell at the corner where the parrnd-mine, parrnd-mine-inv, and sipo-mine-inv cells meet. Array the sipo-mine-out cell 1 high by m long.

6. Place a sipo-mine-cell directly on top of the left most sipo-mine-out cell and array it n-1 high by m long.

7. Place a sipo-mine-end-cap cell directly on top the upper left sipo-mine cell and array it 1 high by m long.

Appendix C

Tiny Chip Test Plans

C1. Multiplier Test Cells Tiny Chip

C1.1 Introduction

The multiplier test cells tiny chip contains separate instances of each of the subcells required for basic WFTA multiplier operations as well as a sample 8-stage ring counter with a PLA. It is also wired such that an input pad is connected directly to an output pad. In all, there are nine different functional areas tested as listed in tables 4.10 and 4.11 and each area was designed to be tested in accordance with section 4.5.

C1.2 DC Tests

To perform the required DC tests on this chip, input pads IZ00 through IZ19 should be connected to ground through similarly sized transistors and the procedures of section 4.5.2 should be followed. First the main power should be used to test for chip latch up, then each of the individual test cell Vdd inputs should be used one at a time. These inputs are IZ00, IZ01, IZ03, IZ04, IZ08, IZ18, and IZ19.

1.3 Functional Tests

1.3.1 Pad Test. The first test to be accomplished should be the Input/Output Pad Test (table 4.11, test-M). This test will show the response charactoristics of the input/output pads as the limiting factor in how fast the test equipment can be operated.

This test consists of inputing a bit stream through IZ16 and sensing the output of OZ07. The output should be the complement of the input as the input pads are not buffered and the output pads are inverting.

Using the DAS 9200, the response time of the output pads can be determined by sweeping the point in time when data is acquired. In a typical sweep, if the acquisition point is close to the stimulus point, numerous errors will occur but will gradually diminish until only expected outputs are seen. The point where the errors cease is the minimum period required for pad operations. Since subcell inverters will be driving these pads, this period should be doubled for other testing.

1.3.2 Multiplier cell tests. There are five individual multiplier cells tested on this chip as shown in table 4.10. Each cell is isolated from all others through the use of individual power pins. Suitable test vectors and patterns can be generated through the esim simulation of individual cells.

To get the maximum operating frequency of each cell, the PQ1 clock pulse should be stepped toward the PQ2 pulse until test failures result. From the last success, the maximum frequency can be calculated using the procedure found in section 2.3.2.3.

1.3.3 Auxillery cell tests. There are two auxillery cells associated with multiplication. These two cells are

tested using test-J and test-K of table 4.11.

The expected outputs of test-J are just the inverted signals of clocks PQ1 and PQ2, while the expected outputs for test-K are shown in table C1.1.

Table C1.1: Test pattern used to test the mult-mine-end-cap cell.

Input	Output			
1	1X10XX	Input:	control	(IZ13)
1	101011			
1	101011	Output:	rstdc	(OZ10)
0	010100		SE	(OZ11)
1	111011		rstc	(OZ12)
1	101011		rst	(OZ13)
			control-out	(OZ14)
			SEc	(OZ15)

To get the maximum operating frequency of each cell, the PQ1 clock pulse should be stepped toward the PQ2 pulse until test failures result. From the last success, the maximum frequency can be calculated using the procedure found in section 2.3.2.3.

1.3.4 Eight stage controller. This circuit was included as space allowed. The circuit uses the main chip power pins for its Vdd. Since the only inputs to the controller are chip Vdd and the PQ1 and PQ2 clocks, the two output signals must be observed relative to each other. The SDpiso signal changes state each clock cycle, while the outcontrol signal is high every eighth clock cycle, but only at the same time as the

SDpiso signal.

To get the maximum operating frequency of each cell, the PQ1 clock pulse should be stepped toward the PQ2 pulse until test failures result. From the last success, the maximum frequency can be calculated using the procedure found in section 2.3.2.3.

C2. Register Tiny Chip

C2.1 Introduction

The register tiny chip contains single complete four-bit by four-word SIPO and PISO registers as well as the individual cells broken out such that each is isolated from the others and individual tests are possible.

C2.2 DC Tests

To perform the required DC tests on this chip, input pads IZ00 through IZ20 should be connected to ground through similarly sized transistors and the procedures of section 4.5.2 should be followed. First the main power should be used to test for chip latch up, then each of the individual test cell Vdd inputs should be used one at a time. These inputs are IZ12, IZ18, IZ20, and IZ20.

C2.3 Functional Tests

C2.3.1 PISO register test. This test will show the functionality and response times for a sample PISO register. The register consists of one four cell column of piso-mine-ext cells, a three by four array of piso-mine cells, and a four cell column of parzer-mine cells. These cells are also bordered by the correct clock inverter and end-cap cells to form a fully functional and independent sample register.

A recommended intial test pattern for use with the DAS 9200 is given in table C2.1.

Table C2.1: PISO Register Test Vector Pattern.

Control	Data	Output	Control	Data	Output
0100000	1111	XXXX	0100000	0111	1010
1010000	1111	XXXX	1000100	0111	0000
0010000	0000	XXXX	0010100	0111	0000
1010000	0000	XXXX	1010000	0111	1111
0010000	1111	XXXX	0010000	0111	1111
1010000	1111	XXXX	1010000	0111	1111
0010000	0000	XXXX	0010000	0111	1111
1010000	0000	XXXX	1010000	0111	1111
0100000	1010	XXXX	0100000	1000	1111
1010000	1010	0101	1000100	1000	0000
0010000	0101	0101	0010100	1000	0000
1010000	0101	0101	1010000	1000	1111
0010000	1010	0101	0010000	1000	1111
1010000	1010	0101	1010000	1000	0000
0010000	0101	0101	0010000	1000	0000
1010000	0101	0101	1010000	1000	0000
0100000	0101	0101	0100000	1111	0000
1010000	0101	1010	1000100	1111	0000
0010000	1010	0101	0000100	1111	0000
1010000	1010	1010	1000100	1111	0000
0010000	0101	0101	0000100	1111	0000
1010000	0101	0101	1010100	1111	0000
0010000	1010	0101	0010000	1111	0000
1010000	1010	0101	1010000	1111	0000
0100000	1111	0101	0100000	XXXX	1111
1010000	1111	0101	1000100	XXXX	0000
0010000	1111	1010	0000100	XXXX	0000
1010000	1111	0101	1000100	XXXX	0000
0010000	1111	1010	0000100	XXXX	0000
1010000	1111	1010	1010100	XXXX	0000
0010000	1111	1010	0010000	XXXX	1111
1010000	1111	1010	1010000	XXXX	1111

Control Word		Data Word		Output Word	
SDpiso	(IZ08)	piso-msb	(IZ00)	data-out-a	(OZ00)
Lpiso	(IZ09)	piso-2	(IZ01)	data-out-b	(OZ01)
SRpiso	(IZ10)	piso-1	(IZ02)	data-out-c	(OZ02)
parchk	(IZ15)	piso-lsb	(IZ03)	data-out-d	(OZ03)
zerofill	(IZ16)				
par-latch	(IZ17)				
OPBAR	(IZ18)				

Note: There is a nine clock cycle delay between the first valid input and the first valid output.

To get the maximum operating frequency of each cell, the PQ1 clock pulse should be stepped toward the PQ2 pulse until test failures result. From the last success, the maximum frequency can be calculated using the procedure found in section 2.3.2.3.

C2.3.2 SIPO register test. This test will show the functionality and response times for a sample SIPO register. The register consists of one four cell column of parzer-mine cells, a four by three array of sipo-mine cells, and a four cell row of sipo-mine-out cells. These cells are also bordered by the correct clock inverter and end-cap cells to form a fully functional and independent sample register.

A recommended intial test pattern for use with the DAS 9200 is given in table C2.2.

C2.3.3 Individual cell tests. Individual cells were placed isolated from each other such that no two cells have the same wells. Due the limited number of input pads available, each group of four cells has the same Vdd. As such, three or four cells are tested at one time. The groupings, as shown in table 4.7, are by overall function.

The expected outputs can be determined by computer simulation or logic analysis.

To get the maximum operating frequency of each cell, the PQ1 clock pulse should be stepped toward the PQ2 pulse until test failures result. From the last success, the maximum

frequency can be calculated using the procedure found in section 2.3.2.3.

Table C2.2: SIPO register test vector pattern.

Control	Data	Output	Control	Data	Output
11010	0000	XXXX	11010	0110	0010
00010	1010	XXXX	00010	0011	0010
10010	0000	XXXX	10010	1001	0001
00010	1111	XXXX	00010	1100	0001
10110	1111	XXXX	10110	0110	1101
00100	1111	XXXX	00100	0011	1101
10100	0000	XXXX	10100	1001	0100
00001	1111	XXXX	00001	1100	0100
11010	0101	0100	11010	0101	1110
00010	1010	0100	00010	1010	1110
10010	0101	0100	10010	0111	1011
00010	1100	0100	00010	1110	1011
10110	0011	0100	10110	0111	0010
00100	1111	0100	00100	1111	0010
10100	0010	0100	10100	1010	1101
00001	1100	0100	00001	1110	1101
11010	1111	1011	11010	1111	1011
00010	1111	1011	00010	1111	1011
10010	1111	0111	10010	1111	1000
00010	1111	0111	00010	0000	1000
10110	1111	0010	10110	1111	0100
00100	1111	0010	00100	1111	0100
10100	1111	0010	10100	1111	0110
00001	1111	0010	00001	XXXX	0110
11010	1111	1000	11010	XXXX	1111
00010	0000	1000	00010	XXXX	1111
10010	1000	1000	10010	XXXX	1111
00010	0100	1000	00010	XXXX	1111
10110	0010	1000	10110	XXXX	1111
00100	0001	1000	00100	XXXX	1111
10100	1100	1000	10100	XXXX	0000
00001	0110	1000	00001	XXXX	0000

Control Word		Data Word		Output Word	
SDsipo'	(IZ08)	sipo-3	(IZ03)	data-out-a	(OZ11)
Lsipo	(IZ11)	sipo-2	(IZ02)	data-out-b	(OZ12)
rcalc	(IZ12)	sipo-1	(IZ01)	data-out-c	(OZ13)
pcalc'	(IZ13)	sipo-0	(IZ00)	data-out-d	(OZ14)
par-append	(IZ14)				

C3. Preadd Test Tiny Chip

C3.1 Introduction

This chip was designed to test a complete WFAT16 preadd section as well as each of the four individual cells required for full adder operations. In all, there are five functional areas to be tested as shown in tables 4.8 and 4.9.

C3.2 DC Tests

To perform the required DC tests on this chip, input pads IZ00 through IZ11 should be connected to ground through similarly sized transistors and the procedures of section 4.5.2 should be followed. First the main power should be used to test for chip latch up, then each of the individual test cell Vdd inputs should be used one at a time. These inputs are IZ08, IZ09, IZ10, and IZ11.

C3.3 Functional Tests

C3.3.1 Preadd section test. This test will show the functionality and response time for an entire WFTA16 preadd section. Due to the limited number of input pins available, some input signals were drawn off the same input pin as shown in table 4.8, but since the odd preadd inputs and the even inputs do not affect the same outputs, this is not a problem.

Table C3.1 gives an initial set of test vectors to be used with the DAS 9200. Additional test vectors can be generated using computer simulations.

Table C3.1: Preadd section test vector pattern.

Control	Input	Output	Control	Input	Output
0	000000000	XXXXX	1	000111100	18EB2
1	111100000	XXXXX	1	111100001	15E77
1	111100000	XXXXX	1	111100001	6AF49
1	000011111	0C13F	1	000011111	14740
1	100011111	6245B	0	000011111	62E6C
1	100011111	6C477	1	111111111	6D46C
1	100011001	6058F	1	111111111	1D2AC
1	100011001	035B3	1	111111111	7FFFF
1	100011001	01593	1	111111111	7FFFF
1	110110001	065FF	1	111111111	7FFFF
1	110110001	075FF	1	111111111	7DFF7
1	110110001	7BAC1	1	111111111	7FDF7
0	011000010	76667	1	111111111	7DFF7
1	111011010	7E667	1	111111111	7DFF7
1	111011010	0295A	1	111111111	7DFF7
1	111011010	7C1FC	1	111111111	7FDF7
1	111011010	79C74	0	111111111	7DFF7
1	111011010	7FDFC	1	111111111	7DFF7
1	111011010	7DDF4	1	000000000	7DFF7
1	111011010	7DDF4	1	111111111	7FFFF
1	111011010	7DDF4	1	000000000	7FFFF
1	111011010	7DDF4	1	111111111	7FFFF
1	111011010	7DDF4	1	000000000	7DFF7
1	111011010	7DDF4	1	000000000	7FFFF
0	000000101	7DDF4	1	111111111	7DFF7
1	000000101	7DDF4	1	000000000	7FFFF
1	000000101	72C0A	1	111111111	7DFF7
1	000000101	73002	1	111111111	7FFFF
1	000000101	71213	0	111111111	7FFFF
1	000000101	71213	1	000000000	7DFF7
1	000000101	71213	1	000000000	7FFFF
1	000000101	71213	1	000000000	7FFFF
1	000000101	71213	1	000000000	7FFFF
1	000000101	71213	1	000000000	7FFFF
1	000000101	71213	1	000000000	7FFFF
1	000000101	71213	1	000000000	7FFFF
0	111111111	71213	1	000000000	7FFFF
1	011111111	71213	1	000000000	7FFFF
1	101111111	7DDEE	1	000000000	7FFFF
1	110111111	000C7	1	000000000	7FFFF
1	111011111	715EF	1	000000000	7FFFF
1	111101111	024C9	1	000000000	7FFFF
1	111111101	6AF49	1	000000000	7FFFF
1	111111101	15B57			

The composition of the control, input, and output words are as follows:

Control =	reset-in		(IZ00)	Outputs =		OZ05	OZ06	OZ07
					OZ08	OZ09	OZ10	OZ11
Input =	h5	h14	(IZ01)		OZ12	OZ13	OZ14	OZ15
	h13		(IZ02)		OZ16	OZ17	OZ18	OZ19
	h4	h11	(IZ03)		OZ20	OZ21	OZ22	OZ23
	h12	h15	(IZ04)					
	h3	h10	(IZ05)					
	h2	h9	(IZ08)					
	h1	h8	(IZ09)					
	h0	h7	(IZ10)					
	h6		(IZ11)					

To get the maximum operating frequency of each cell, the PQ1 clock pulse should be stepped toward the PQ2 pulse until test failures result. From the last success, the maximum frequency can be calculated using the procedure found in section 2.3.2.3.

C3.3.2 Individual cell tests. The four cells required for complete adder operations can be tested individually by setting only one of the IZ08 through IZ11 pads high, while keepint the other three low. This turns only one subcell on, while keeping the other three off. The inputs and outputs are shown in table 4.9. Test patterns can be generated either through computer simulation or logic analysis.

To get the maximum operating frequency of each cell, the PQ1 clock pulse should be stepped toward the PQ2 pulse until test failures result. From the last success, the maximum frequency can be calculated using the procedure found in section 2.3.2.3.

C4. Multiplier Interface Tiny Chip

C4.1 Introduction

This chip was designed to test every multiplier cell and its interfaces with every other multiplier cell. The chip was designed such that every set of multiplier cells is tested in a single test as shwn in table 4.12.

C4.2 DC Tests

To perform the required DC tests on this chip, inputs pads IZ00 through IZ04 should be connected to ground through similarly sized transistors and the procedures of section 4.5.2 should be followed.

C4.3 Functional Test

This test will show the functionality and operational frequency of a subset of the WFTA multiplier section. Each of the multiplier outputs comes from the partial product results, while the data signal is output to probe pads.

Table C4.1 gives an initial set of test vectors to be used with the DAS 9200. Additional test vectors can be generated using computer simulations.

To get the maximum operating frequency of each cell, the PQ1 clock pulse should be stepped toward the PQ2 pulse until test failures result. From the last success, the maximum frequency can be calculated using the procedure found in section 2.3.2.3.

Table C4.1: Multiplier Interface Tiny Chip Test Pattern

Input	Output	Input	Output	Input	Output
XX0	XXXXXXX				
001	XXXXXXX	111	3E2C02B	001	1C994DA
001	XXXXXXX	111	3E2C02B	001	09B1ECE
001	XXXXXXX	111	3E2C02B	001	27B2714
001	XXXXXXX	111	3E2C02B	001	1AC384D
001	XXXXXXX	111	3E2C02B	001	1AC384D
001	XXXXXXX	111	3E2C02B	001	1AC384D
001	3FFFFFF	111	1B43F64	001	3FFFFFF
001	3FFFFFF	111	0163FE4	001	3FFFFFF
001	3FFFFFF	111	0163FE4	001	3FFFFFF
000	3FFFFFF	110	0163FE4	001	3FFFFFF
101	3FFFFFF	001	0163FE4		
101	3FFFFFF	111	3E9C01B		
101	3FFFFFF	001	3F9FF00		
101	3FFFFFF	111	3F9FF00		
101	3FFFFFF	001	3F9FF00		
101	3FFFFFF	111	3F9FF00		
101	0BC3E64	001	2366B25		
101	01E3FE4	111	09B1ECE		
101	01E3FE4	001	2366B25		
100	01E3FE4	110	09B1ECE		
011	01E3FE4	111	2366B25		
011	3E2C02B	001	364E131		
011	0F1F600	111	184D8EB		
011	0F1F600	001	253C7B2		
011	0F1F600	111	253C7B2		
011	0F1F600	001	253C7B2		
011	3E2C02B	111	1C994DA		
011	3E2C02B	001	364E131		
011	3E2C02B	111	1C994DA		
010	3E2C02B	000	364E131		

Input data: multiplicand
partial-product
mult-control

Output data:
OZ00 OZ01 OZ02 OZ03 OZ04 OZ05
OZ11 OZ12 OZ13 OZ14 OZ15 OZ16 OZ17 OZ18
OZ19 OZ20 OZ21 OZ22 OZ23 OZ24 OZ25 OZ26
OZ27 OZ28 OZ29 OZ30

Note: There is a six clock cycle delay between the data input and its expected output.

C5. Postadd Test Tiny Chip

C5.1 Introduction

This chip was designed to test a complete WFAT16 postadd section as well as each of the four individual cells required for full adder operations. In all, there are five functional areas to be tested as shown in tables 4.13 and 4.9.

C5.2 DC Tests

To perform the required DC tests on this chip, input pads IZ00 through IZ13 should be connected to ground through similarly sized transistors and the procedures of section 4.5.2 should be followed. First the main power should be used to test for chip latch up, then each of the individual test cell Vdd inputs should be used one at a time. These inputs are IZ08, IZ09, IZ10, and IZ11.

C5.3 Functional Tests

C5.3.1 Postadd section test. This test will show the functionality and response time for an entire WFTA16 postadd section. Due to the limited number of input pins available, some input signals were drawn off the same input pin as shown in table 4.13.

Table C5.1 gives an initial set of test vectors to be used with the DAS 9200. Additional test vectors can be generated using computer simulations.

Table C5.1: Preadd section test vector pattern.

Control	Input	Output	Control	Input	Output	Control	Input	Output
0	000	XXXX	1	7E0	F9FA	1	7FF	F2AE
1	000	XXXX	1	01F	5687	1	7FF	F2AE
1	000	XXXX	1	7E0	F9FA	1	7FF	F2AE
1	000	XXXX	1	01F	5687	1	7FF	F2AE
1	000	FFFF	1	7E0	F9FA	1	7FF	F2AE
1	000	FFFF	1	01F	5687	0	7FF	F2AE
1	000	FFFF	1	7E0	F9FA	1	000	F2AE
1	000	FFFF	1	01F	5687	1	000	F2AE
1	000	FFFF	1	7E0	F9FA	1	000	FFFF
1	000	FFFF	1	01F	5687	1	000	FFFF
1	000	FFFF	0	7E0	F9FA	1	000	FFFF
1	000	FFFF	1	7E0	5687	1	000	FFFF
1	000	FFFF	1	01F	F9FA	1	000	FFFF
1	000	FFFF	1	7E0	FFC3	1	000	FFFF
1	000	FFFF	1	01F	5597	1	000	FFFF
0	000	FFFF	1	7E0	F9FA	1	000	FFFF
1	7FF	FFFF	1	01F	5687	1	000	FFFF
1	7FF	FFFF	1	7E0	F9FA	1	000	FFFF
1	7FF	FFFF	1	01F	5687	1	000	FFFF
1	7FF	F06E	1	7E0	F9FA	1	000	FFFF
1	7FF	F3AE	1	01F	5687	0	000	FFFF
1	7FF	F2AE	1	7E0	F9FA	1	000	FFFF
1	7FF	F2AE	1	01F	5687	1	000	FFFF
1	7FF	F2AE	1	7E0	F9FA	1	000	FFFF
1	7FF	F2AE	1	01F	5687	1	000	FFFF
1	7FF	F2AE	0	7E0	F9FA	1	000	FFFF
1	7FF	F2AE	1	7FF	5687	1	000	FFFF
1	7FF	F2AE	1	7FF	F9FA	1	000	FFFF
1	7FF	F2AE	1	7FF	FFFF	1	000	FFFF
1	7FF	F2AE	1	7FF	F06E	1	000	FFFF
0	7FF	F2AE	1	7FF	F3AE	1	000	FFFF
1	7E0	F2AE	1	7FF	F2AE	1	000	FFFF
1	01F	F2AE	1	7FF	F2AE	1	000	FFFF
1	7E0	FFC3	1	7FF	F2AE	1	000	FFFF
1	01F	5597	1	7FF	F2AE	1	000	FFFF

The composition of the control, input, and output words are as follows:

Control =	reset-in		(IZ00)	Outputs =	OZ08	OZ09	OZ10	OZ11
					OZ12	OZ13	OZ14	OZ15
Input =	t3	t11	(IZ01)		OZ16	OZ17	OZ18	OZ19
	t5		(IZ02)		OZ20	OZ21	OZ22	OZ23
	t2	t15	(IZ03)					
	t6	t10	(IZ04)					
	t12	t16	(IZ05)					
	t17		(IZ08)					
	t8	t14	(IZ09)					
	t7		(IZ10)					
	t9		(IZ11)					
	t0	t4	(IZ12)					
	t1	t13	(IZ13)					

To get the maximum operating frequency of each cell, the PQ1 clock pulse should be stepped toward the PQ2 pulse until test failures result. From the last success, the maximum frequency can be calculated using the procedure found in section 2.3.2.3.

C5.3.2 Individual cell tests. The four cells required for complete adder operations can be tested individually by setting only one of the IZ08 through IZ11 pads high, while keepint the other three low. This turns only one subcell on, while keeping the other three off. The inputs and outputs are shown in table 4.9. Test patterns can be generated either through computer simulation or logic analysis.

To get the maximum operating frequency of each cell, the PQ1 clock pulse should be stepped toward the PQ2 pulse until test failures result. The maximum frequency can be calculated using the procedure found in section 2.3.2.3.

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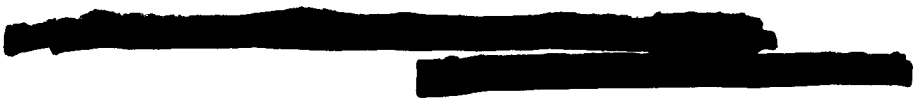
Vita

Captain Steven Pavick, [redacted] graduated from Cupertino High School, Cupertino, California in 1976. He enlisted as an Airman Basic in the United States Air Force on 17 December 1979 after having attended De Anza Community College, Cupertino, California and having worked various jobs to support his education. After graduation from the Basic Military Training School, Lackland AFB, Texas, he was assigned to Lowry AFB, Colorado for technical training into the Scientific Measurement Technician career field. Upon completion of training, as a distinguished graduate, Captain Pavick was assigned, as an Airman, to the Air Force Technical Applications Center (AFTAC) Detachment 421 in Alice Springs, Austrailia, where he met and married his wife Sussan. When he returned to the United States in 1982, Captain Pavick, as an Airman First Class, was assigned as a general computer programmer at Headquarters AFTAC, Patrick AFB, Florida, where his duties included generating application software using assembly, fortran, cobol, and PL1 programming languages. While at Headquarters AFTAC, he continued his education through Rollins College, Winter Park, Florida and worked toward a Bachelors of Math Science degree until he accepted an Airman Education and Commissioning Program (AECP) electrical engineering scholarship. As a Staff Sergeant in the AECP scholarship program, Captain Pavick enrolled in the

University of Central Florida, College of Engineering, in January 1983 and graduated with a Bachelor of Science in Engineering degree in December 1984. Immediately after graduation, he was sent to the Air Force Officer Training School (OTS), Lackland AFB, Texas. He graduated from OTS and received a commission as a Second Lieutenant in the United States Air Force on 5 April 1985. After a three year tour with the 554 Range Group, Nellis AFB, Nevada, performing radar engineering and contract management duties, he entered the Air Force Institute of Technology, School of Engineering, in May 1988 where he studied the design and testing of very large scale and very high speed integrated circuits as well as electronic device technology. Captain Pavick graduated from AFIT in December 1989 with a Masters of Science in Electrical Engineering degree.



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Abstract

A prototype 16-point, 70 MHz Fourier transform processor using 1.2 micron minimum feature sizes was tested using a Tektronix DAS 9200, digital analysis system. The results showed that it is possible to operate an Air Force Institute of Technology (AFIT) WFT16 chip at 70 MHz. The results also showed a great deal of variation among the individual packaged chips. Using the WFT16's built in testing circuitry, portions of the main data and control circuitry were tested. The AFIT XROM address generator and control circuitry proved to be the most reliable chip subsection, followed by the arithmetic and register control section. The parallel-in serial-out input data register was also tested and showed consistent results even though the results were not as expected. The variation among chips was shown when attempts at trivial transforms were done. The attempted transforms consisted of DC data values of zero and minus one. Two of 16 tested chips showed correct transform values, but for only a limited, nonrepeated sequence. In later testing, two chips were found that gave repeatable results which closely approximated the expected results for both trivial and nontrivial transform attempts. Test procedures and input to output relationships were determine to aid further testing of the AFIT WFT16 circuit.